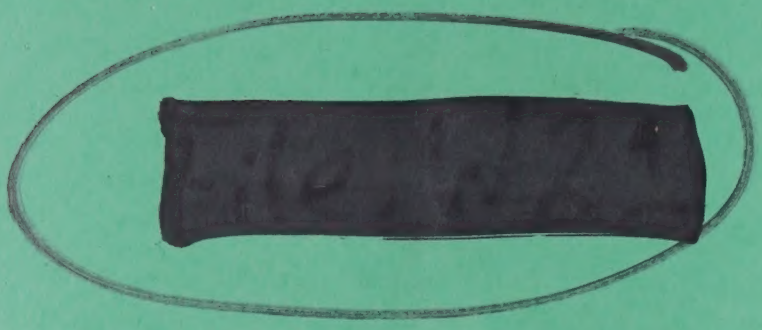
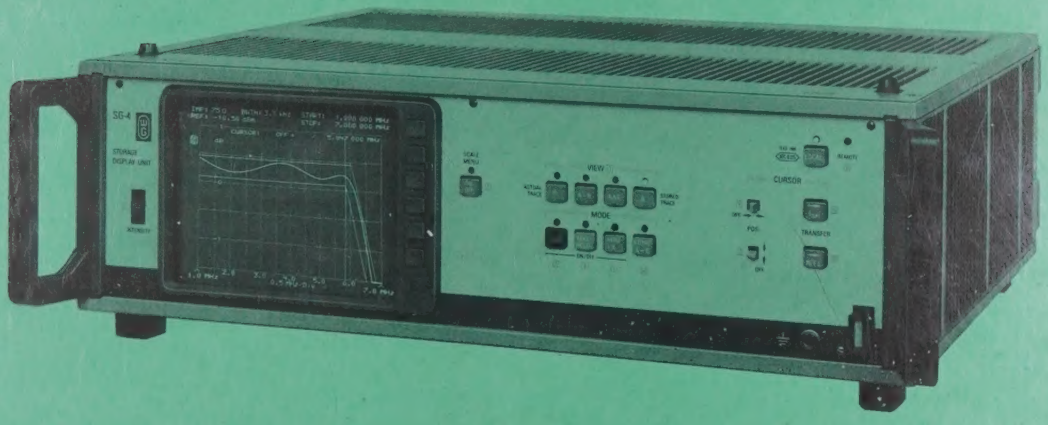
Service Manual





Display Unit

SG-4

with digital image storage for use with the SPM-16 and SPM-19 Selective Level Meters

BN 0957/00.83; Series A...

DISPLAY UNIT SG-4

with digital image storage for use with the
SPM-16 and SPM-19 Selective Level Meters

Service Manual BN 957; Series A...

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PRECISION ELECTRONIC
MEASURING INSTRUMENTS

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6 PRELIMINARY REMARKS

6.1 OVERVIEW OF THE SERVICE PROCEDURE

The time taken to detect faults and carry out repairs should be as short as possible. Various service aids have been provided to help you find defective assemblies quickly.

Instruments with microprocessor control have an automatic test for the digital section. Further test programs like the hardware self-test are provided, and give you a rough idea where the fault is without having to dismantle the instrument. As far as possible, error numbers or signs are used to indicate which functional unit is faulty.

The next step is signature analysis which allows you to check the control unit when the microprocessor is in free run mode. If the CPU is o.k., a DIL switch on the CPU board can be used to call up further test routines and signature stimuli for other circuits. If signature analysis is not successful the board in question must be replaced.

Basically the procedure for troubleshooting the analog section is no different from that for checking the digital section.

It should be possible to guess which assembly is faulty from the behaviour of the instrument (power supply, decade switches etc.). Important information about the location of faulty assemblies is given by important signals like regulation voltages, levels, power supply etc.

A monitor program is provided as an aid if the instrument is microprocessor controlled.

This software is used to bring the instrument into certain well-defined states (attenuators, amplifiers etc). The monitor is either provided with the other instrument software or is available as a separate service EPROM.

If one wishes to localise faulty components on boards or in subassemblies, the Appendix and the circuit descriptions given in this Service Manual (chap.9) can be used for troubleshooting. Chapter 7 provides more information about troubleshooting and alignment.

6.2 SERVICE AIDS

6.2.1 TEST PROGRAMS

The SG-4 has test programs to give a quick overview of how the instrument is functioning. The digital section is tested automatically when the power is switched on (POWER ON). This involves carrying out a "non-destructive" test in the RAM. All the data, parameters, setup etc. remain unmodified in memory.

Hardware self-tests can be carried out on instruments with internal signal sources (calibration source, built-in generator) and detectors (e.g. A/D converters). The limited number of detectors means that this is only an approximate procedure.

The guaranteed data must always be checked with external instruments and standards. As the instrument has an IEC bus and so has a remote control capability this kind of testing can be carried out automatically.

Special test programs are available to help you test instruments with a wide range of setting parameters and measuring functions on a rational basis. Contact your customer bureau for more information.

6.2.2 SERVICE SWITCH

CPU-2/BN 965 has a ten pole DIL switch. Switches S1/7 - 1/10 are required to put the microprocessor in free-run mode. Switches S1/1 - S1/6 form the acutal service switches. This switch can form all binary numbers between 0 and 63.

Definition: 0 = switch OFF (open)
1 = switch ON (closed)

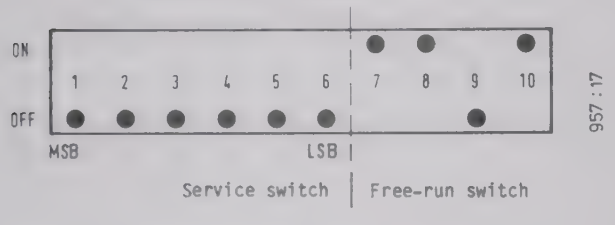


Figure 6-1 Service switch (normal operation)

In normal mode (measurement mode) only switches S1/7, S1/8 and S1/10 are closed. Service programs, such as cyclic tests, one-off tests and stimulus programs, can be called up with the service switch. The code that has been set causes the processor to determine the program start address in a table during initialisation (i.e. after POWER ON or CLEAR).

Afterwards, the test or stimulus program is carried out once or repeated.

A 6 bit word can be set on the service switch.

Switch	S1/1	S1/2	S1/3	S1/4	S1/5	S1/6
value	32	16	8	4	2	1

*N.B. important!

Status definition for the service switch for SG-4:
0 = switch OFF (open)
1 = switch ON (closed)

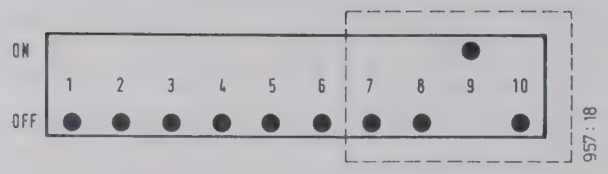
As well as the fact that negative logic is used, the user should also note that the bit pattern is inverted.
MSB = S1/1
LSB = S1/6

6.2.3 FREE RUN MODE SWITCH

The free-run mode switch is the switch array on the right half of the DIL switch on CPU board (S1/7, S1/10).

The free-run mode switch is only required for signature analysis on the CPU (ROM and RAM). The free-run mode switch is only set as shown below when signature analysis is carried out.

Definition: 0 = switch OFF (open)
1 = switch ON (closed)



Free-run switch

Figure 6-2 Free run switch set for signature analysis

If the switches S1/7 to S1/10 are switched back the CPU operates normally again.

6.2.4 SIGNATURE ANALYSIS

Digital signal sequences of any length can be checked reliably and quickly with a signature analyzer (e.g. hp 5004A/5005A). Each line to be tested has a constant signature (4 digits, quasi hexadecimal), if a well-defined, repeatable bit pattern is available and can be referred to a time window (STOP/START frame). The microprocessor is forced to produce bit patterns of this kind by the stimulus programs or external circuitry.

The CPU board has a free-run mode switch for carrying out signature analysis (S1/7 - S1/10).

If switches S1/7 - S1/10 are set to the opposite position, and RESET pressed the microprocessor addresses each address in the memory area in turn and repeats this process cyclically. To record ROM signatures, the relevant ROM select (test point) must be used as the Start/Stop signal. The free-run mode switch, the pull-up resistors of the data line and G12 ensure that only part of the 8085 instruction set is carried out.

Bit	7	6	5	4	3	2	1	0
	H	L	X	X	X	X	X	H

H = high
L = low
X = don't care

NOTE: The free-run mode switch only affects data lines Ø, 6 and 7.

The instructions in question are one byte arithmetic or logical instructions that increment the program counter by one and so give a "program" that addresses each element in the memory.

If the most significant address bit A15 is used as the time window (= START/STOP frame), and if the processor passes through the whole address area (ØØØØH to FFFFH), each address line has a unique signature.

In the case of the 8085 microprocessor, RD is used as the clock signal. The timing of the signals CLOCK, DATA, START and STOP must be absolutely correct as otherwise unstable signatures will result. Two common signatures will be discussed below.

The signature for the 0 V line does not depend on the START/STOP frame and is always 0000. The signature of the +5 V line is called the CHARACTERISTIC SIGNATURE. The characteristic signature shows if the START/STOP frame is correct. One can also assume that the µP is functioning correctly.

If the characteristic signature appears on an address line or data line this means that the line is connected to the supply voltage: If the signature 0000 is detected it means the line is connected to ground.

If two address lines or two data lines have the same signature it is very probable that there is an electrical contact between them. If the address area is restricted to the ROM area in the free-run mode (START/STOP frame corresponds to the relevant chip select signal) a bit sequence signal appears on the data lines, and this sequence gives the ROM contents in the address area in question.

As well as the non-permanent data in the ROM, the contents in the RAM and in the I/O depend on the current "state" of the test instrument. To obtain meaningful signatures one must write well-defined data to the RAM and periodically interrogate the I/O ports. This function is fulfilled by a program called the stimulus program. Programs of this kind as called up via the service switch on the CPU board.

When the SG-4 is switched on or RESET, the µP runs the bootstrapping routine. When this is being carried out the switch positions of S1/1 - S1/6 are interrogated, used to call up certain stimuli and to continue the program from the position so defined.

6.2.5 MONITOR PROGRAM

If one is sure that the control section is functioning correctly (a µP board, I/O ports), a monitor program can be used as a further aid for fault localisation. As well as finding out the type and software status of the instrument, the monitor program supplements various service aids.

On certain instruments e.g. level meters it is possible to interrogate and select certain settings. In this way it is possible to obtain well-defined attenuator and amplifier settings, which are a prerequisite for meaningful level measurements (level plans). These service programs are either part of the instrument software or contained in a separate "Service EPROM".

The required code is set by means of the service switch (S1/1 to S1/6) on CPU-2. By interrogating the service switch during the initialisation phase the correct address for the start of the program can be read from a table.

6.3 MEASURING EQUIPMENT

The equipments listed below are to be thought of as recommendations, equipment from other manufacturers with the same capabilities may also be used.

Measuring equipment	Requirements	Recommended type	Manufacturer	For Use see
Selective Level Meter	IEC 625 INTERFACE BUS	SPM-19* BN 829	W&G	8.2
Level Generator	0 ... -60 dB/dBm	PS-19	W&G	8.2
Digital voltmeter	4 1/2 digits	8600 A	Fluke	8.2
Signature analyser		hp 5004A/ 5005A	hp	

Figure 6-3 Measuring equipment

*) A SPM-16 can be used instead of an SPM-19. The SG-4 can not be used with other level meters.

7 INSTRUCTIONS FOR FAULTFINDING AND REPAIR

7.1 SAFETY MEASURES

7.1.1 PROTECTION FROM ELECTRIC SHOCK

Protection class

This equipment is a unit of Protection Class I according to VDE 0411 or IEC Publication 348. The a.c. power cable supplied contains a ground conductor. The power plug may only be inserted into grounded sockets, except in specially permitted rooms. Any interruption or break in the ground conductor, inside or outside the unit, is not permissible.

Opening the unit

When opening covers or removing parts with tools, live parts can become exposed. Connection points can also be live.

The unit must be disconnected from all voltage sources before it is opened.

If calibration, maintenance or repair on the open unit is then unavoidable with the voltage applied, the operation may only be performed by a skilled person who is aware of the hazards.

Capacitors in the SG-4 can still be charged even when the unit has been disconnected from all voltage sources; the circuit diagrams should be observed for self-protection.

Fuses

Only the specified fuses may be used.

Repairs, replacing parts

Repairs must be performed proficiently. Particular care should be taken not to change the design features of the unit in a manner which may reduce safety. In particular, the creepage paths and air gaps and insulation thicknesses must not be reduced.

Only W & G replacement parts should be used. Other spare parts are only permissible if they do not impare the safety characteristics of the SG-4.

Testing after repairs and maintenance

Testing the ground conductor connection.

Reliability and quality of the connection are tested by visual inspection and by measuring the resistance between the ground conductor terminal at the plug and the housing. The resistance should be $< 0.5\ \Omega$. The connecting cable should be moved to and fro during the measurement. Variations in resistance indicate damage.

Testing the insulation resistance.

Measure the insulation resistance at 500 V d.c. between the a.c. power terminals and the ground conductor terminal. For this purpose, set the power switch of the SG-4 to the "On" position. The insulation resistance should be $> 2\ M\Omega$.

7.1.2 INSTRUCTIONS FOR PROTECTING THE CIRCUITRY

Exercise caution when handling MOS components

Some MOS (metal-oxide-silicon) components are used in this unit. They can be easily destroyed by static charges, noise voltages of ungrounded equipment or other interfering potentials. In order to protect them from static charges, observe the following rules:

- Wherever possible, MOS components should remain in the supplier's packaging until they are required for use. Until this stage, all terminals must remain galvanically interconnected (black, electrically conducting foam).
- Before the MOS components or circuit boards fitted with them are removed, the electrical conducting part of the packaging must make contact with a conducting worktop or the chassis of the SG-4 to be repaired, as reference potential.
- Before touching the MOS components, touch with a hand the conductor which serves as a reference potential.
- All tools, equipment, the section of the unit to be repaired and the person performing the repair should be at the same potential as the conductor which serves as reference potential (e.g. a conducting worktop or, alternatively, the chassis of the equipment to be repaired). For this reason, any tools which will make contact with MOS components must previously make contact with the reference potential. Tools must not have insulated handles.
- In the event of work on a circuit board or other equipment parts which are separated from the rest of the unit, and which are not positioned on a conducting worktop, the ground of the circuit board etc. must be connected to reference potential.

To provide protection against noise voltages during soldering, a permanent connection should be made between the soldering iron and the chassis of the unit to be repaired.

MOS components can be recognized by the letters MOS, CMOS or MOSFET in the component designation of the circuit parts list.

7.1.3 SOLDERING INSTRUCTIONS

It is recommended that small-diameter solder with a low flux content be used. The following should be observed:

- Soldering times for all the components $\leq$ 5 s
- Soldering temperatures $\leq$ 260°
- Avoid splashed flux on switch contacts
- When soldering at switch contacts or other electromechanical components, ensure that no flux creeps onto the contact point.

Instructions for desoldering components with many terminals

The removal of solder from each individual terminal lead by suction, using a special desoldering device is superior to all other methods. When desoldering, ensure that each individual terminal is free by moving it gently to and fro. Do not apply force! Through-plated contacts are sensitive to pulling during soldering! With dual in-line components, harm to the circuit board can be avoided by cutting the connections and desoldering them individually.

7.1.4 UNIT MARKINGS

For queries, ordering spare parts or establishing whether the servicing instructions present pertain to the unit to be repaired, the following unit markings are required:

Type designation, designation of any special version, auxiliary equipment installed, series index and serial number.

Figure 7-1 shows the locations of the individual unit markings.

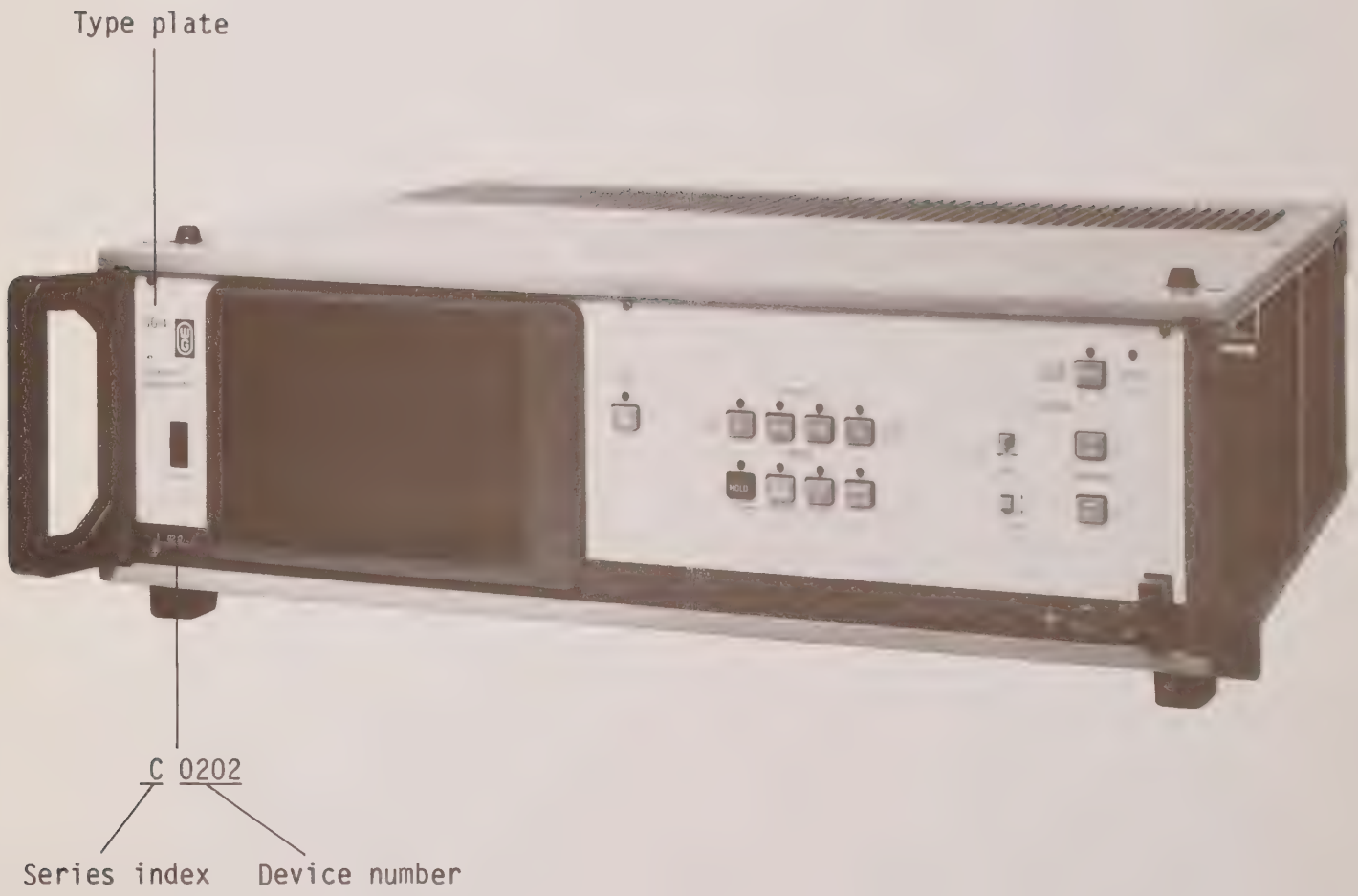


Figure 7-1a Unit markings (front panel)

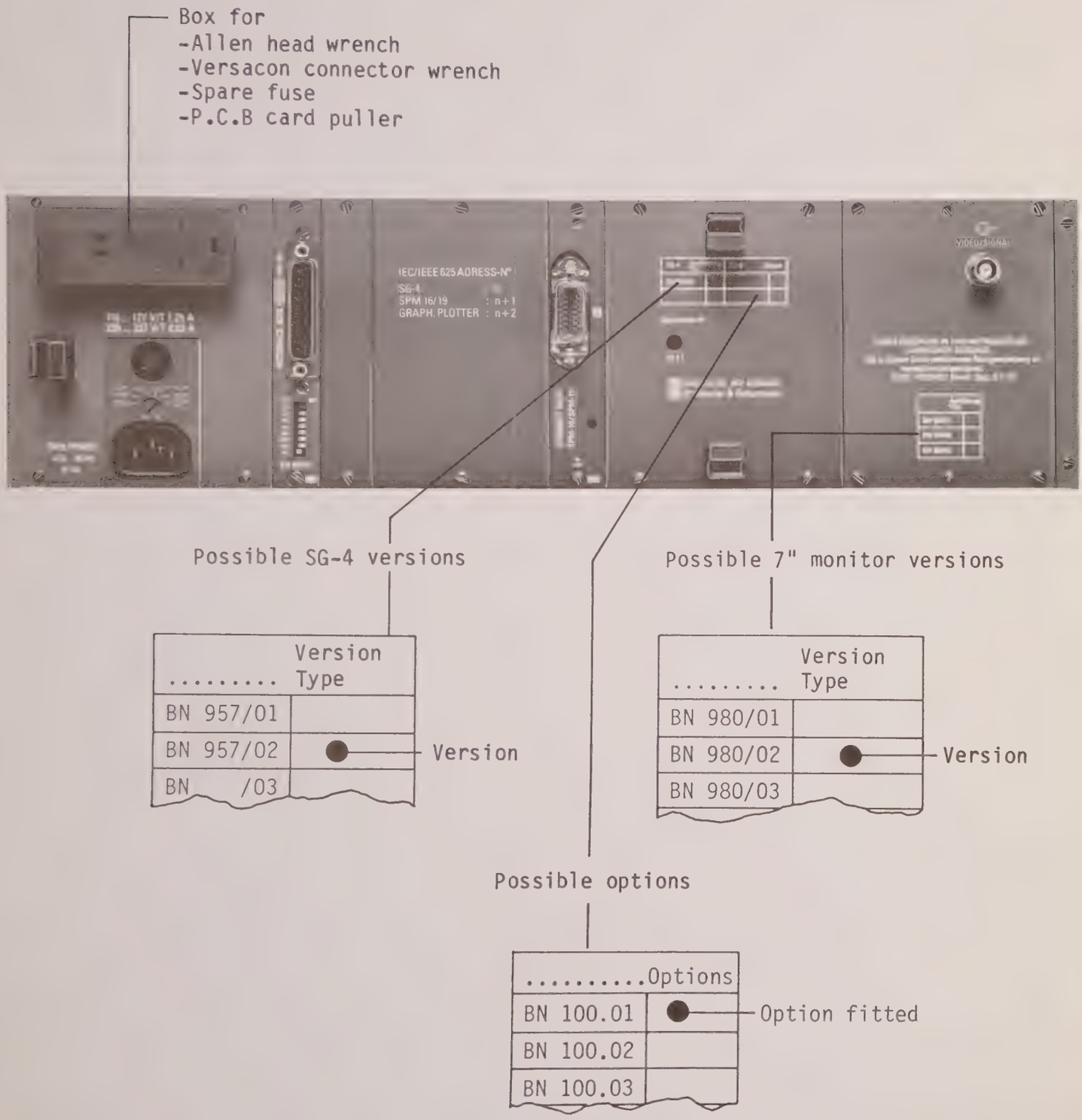


Figure 7-1b Unit markings (back panel)

7.1.5 DISASSEMBLING THE UNIT

See Figure 7-2 for disassembling the SG-4.

After removal of the 6 upper Allen head screws, the instrument is lifted upwards and out from the enclosure. The power supply remains in the enclosure. It is, however, connected to the instrument by a wiring harness.

Tool:
Allen wrench, Sw = 3
(see back panel)

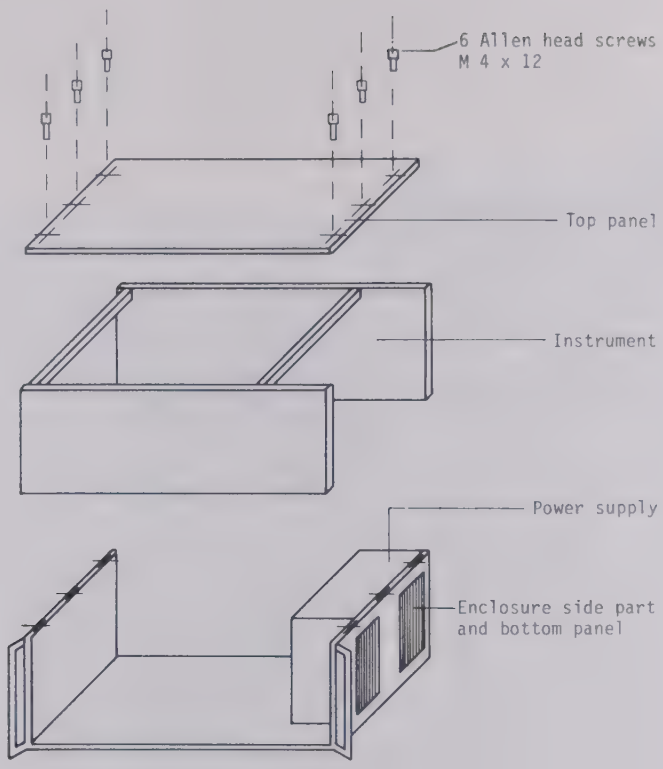


Figure 7-2 Disassembling the SG-4

7.1.6 INITIALIZING THE SOFTWARE

To prevent a possible stoppage of the software, each time that CPU card BN 965 has been removed, the clear function must be initiated after the supply voltage has been switched on. For this purpose, temporarily short-circuit the test surfaces on card BN 965 near the rear of the unit. This also applies after working on the power supply, e.g. changing the batteries.

The clear function can also be initiated by pressing the local key [6] whilst switching on the supply voltage. As a check: the B-curve memory is erased by the clear function.

7.2 ARRANGEMENT OF MODULES, ALIGNMENT ELEMENTS, TEST POINTS

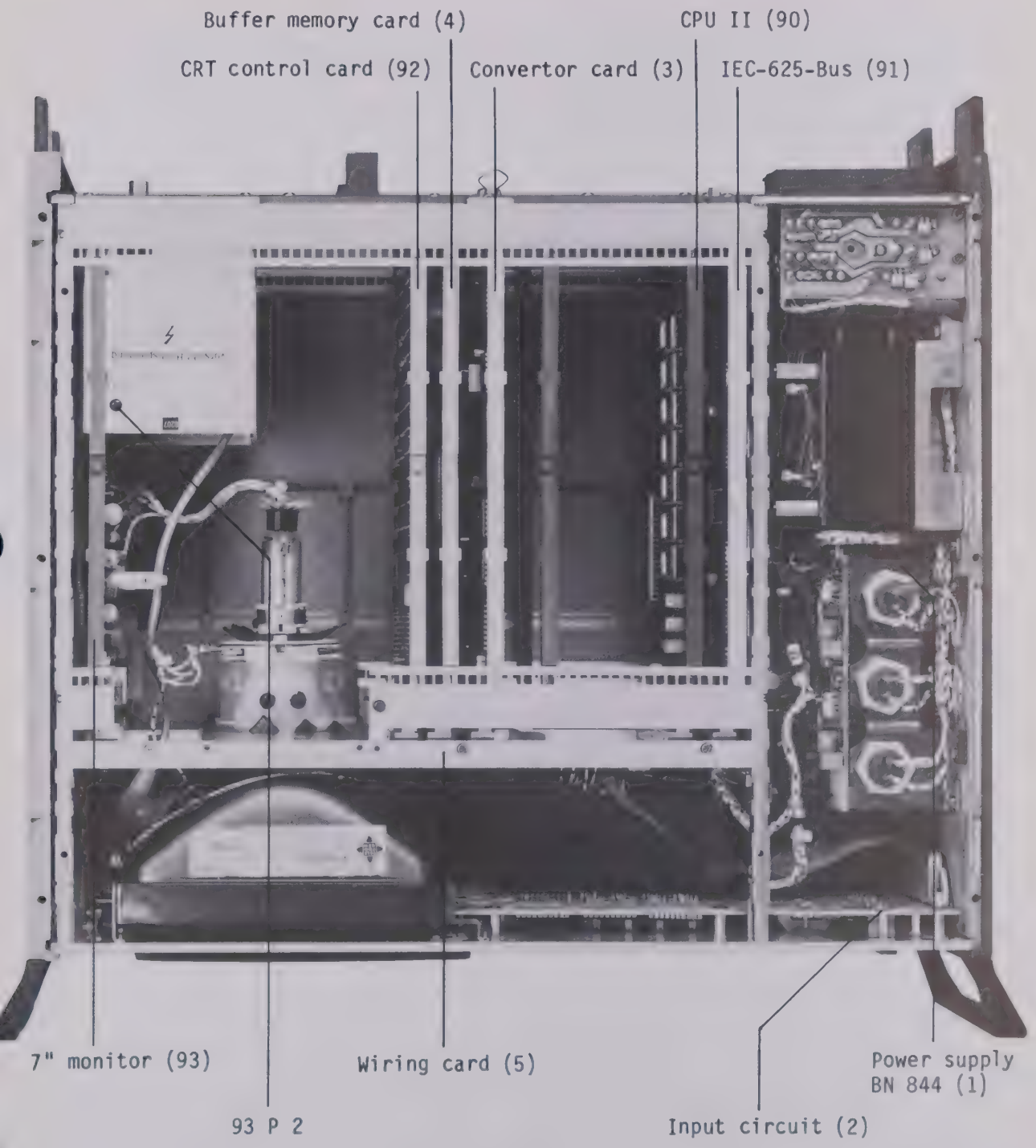


Figure 7-3 SG-4 viewed from above

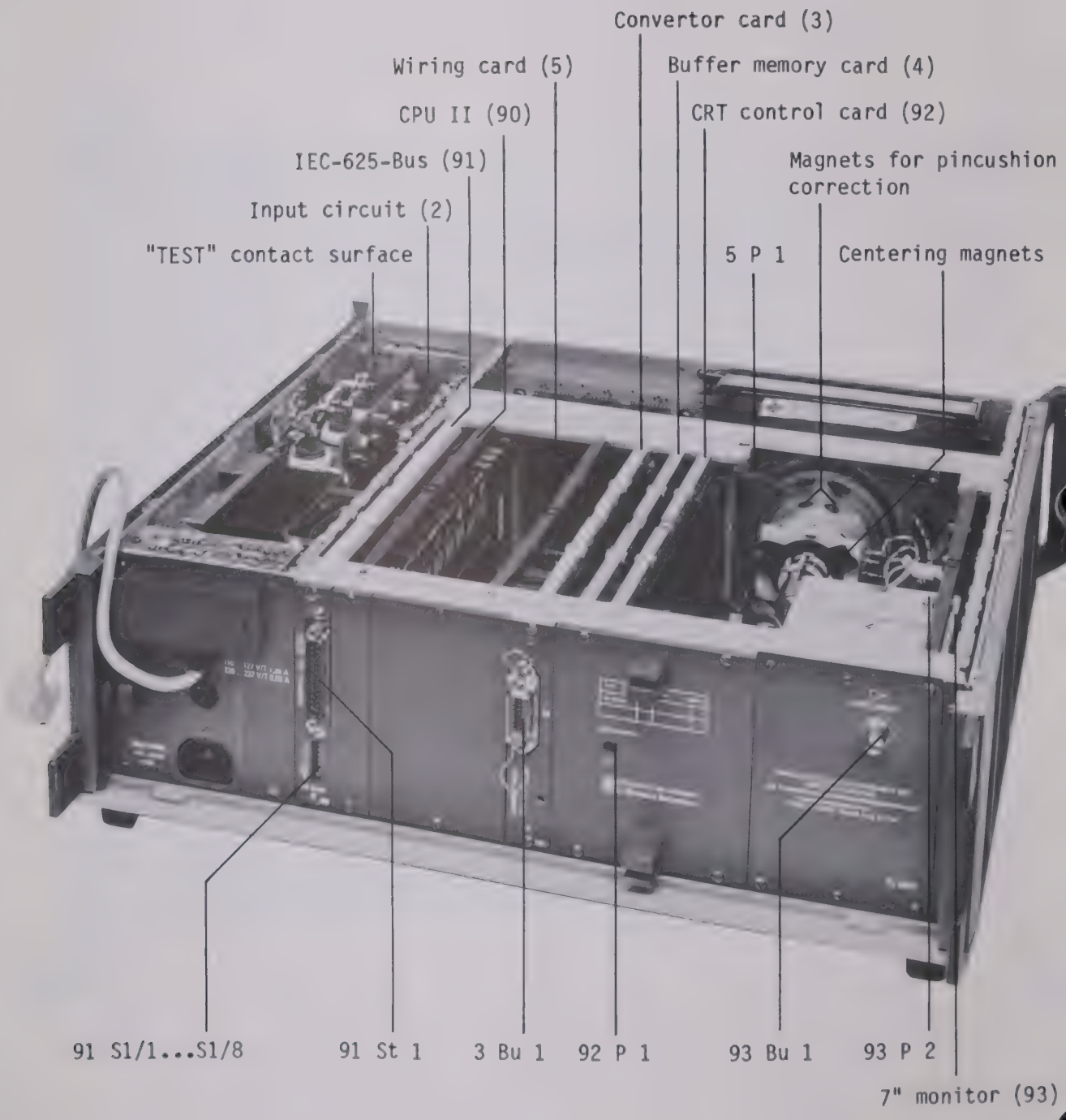


Figure 7-4 SG-4 viewed from the upper rear

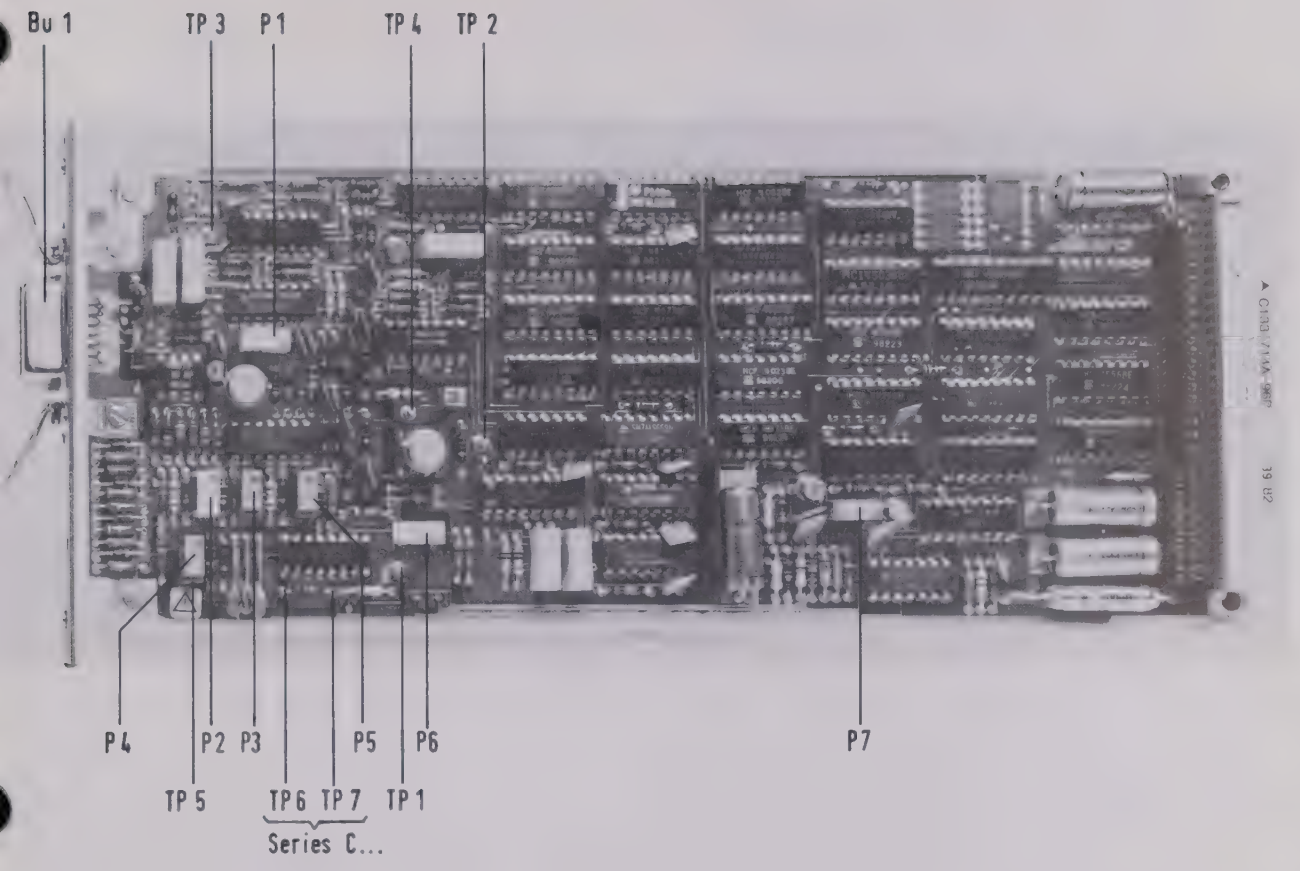


Figure 7-5 Convertor card (3)

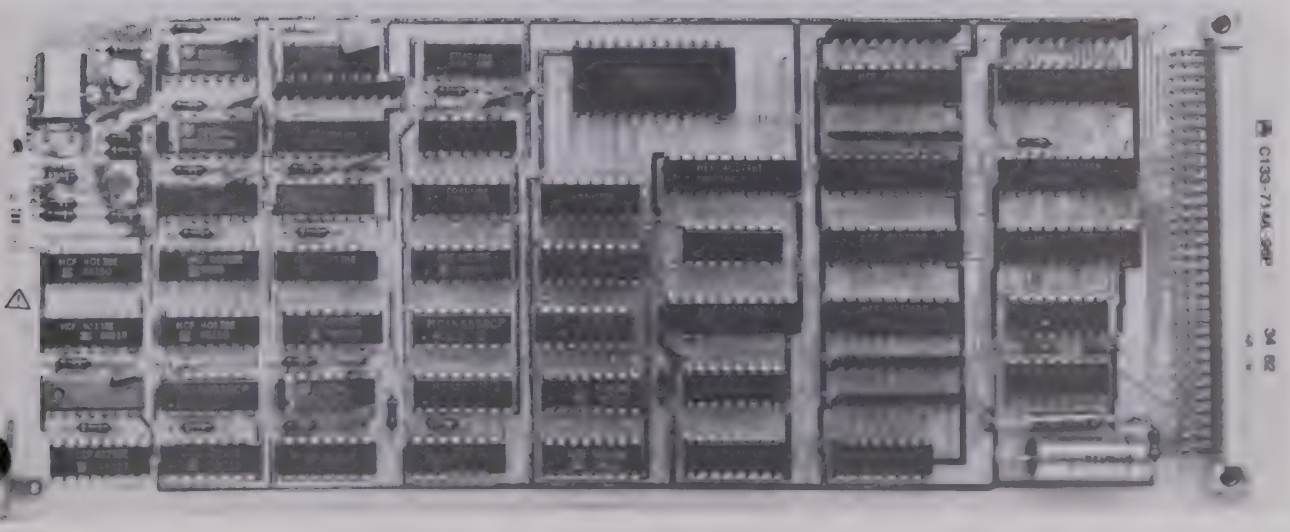


Figure 7-6 Buffer memory card (4)

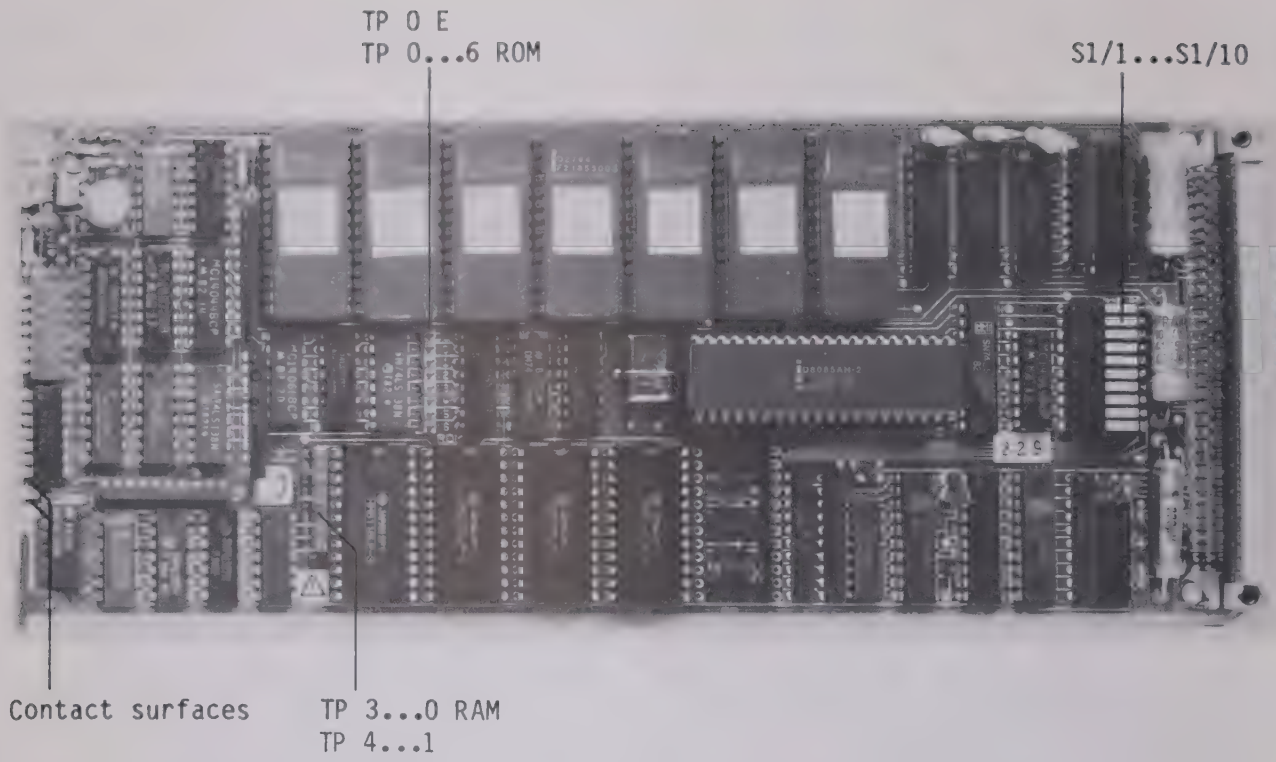


Figure 7-7 CPU II (90) BN 965

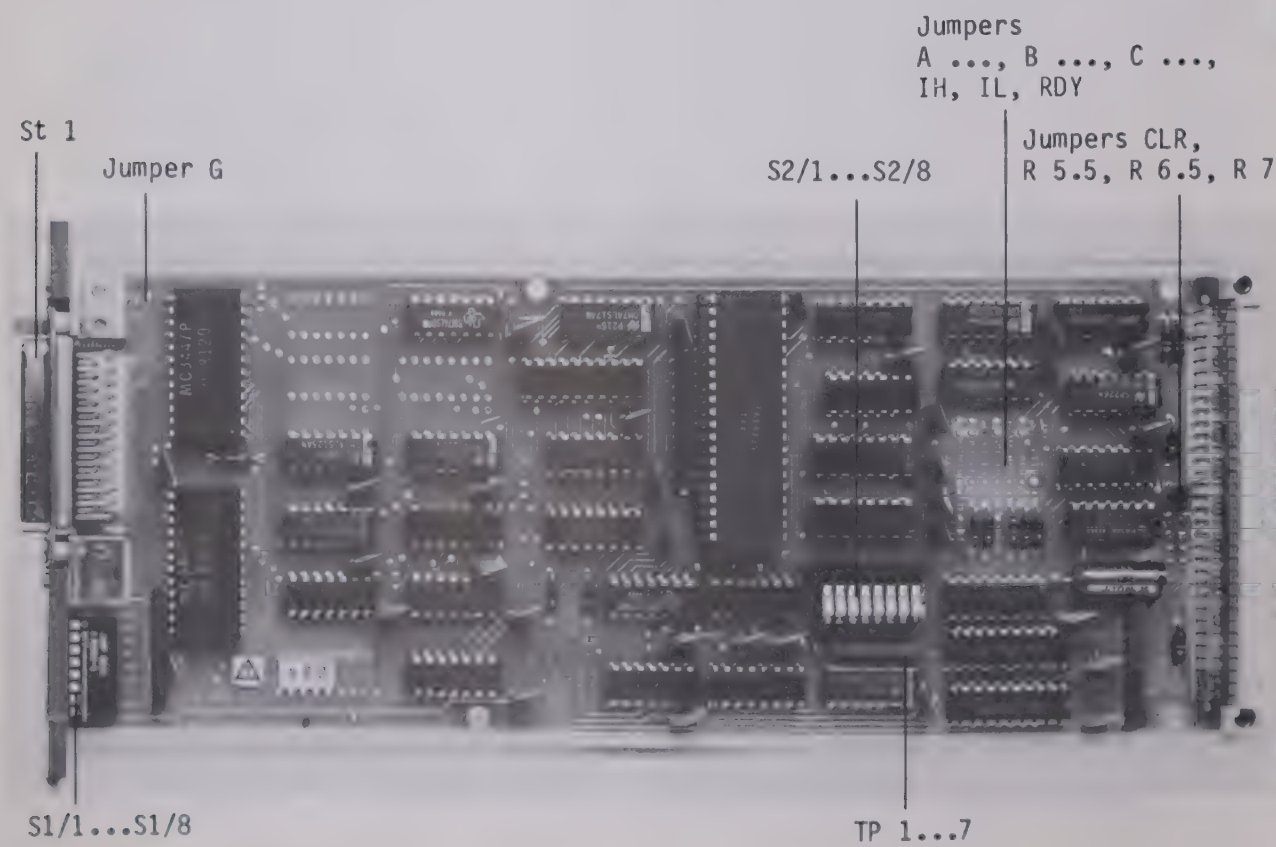


Figure 7-8 IEC-625 bus (91) BN 958

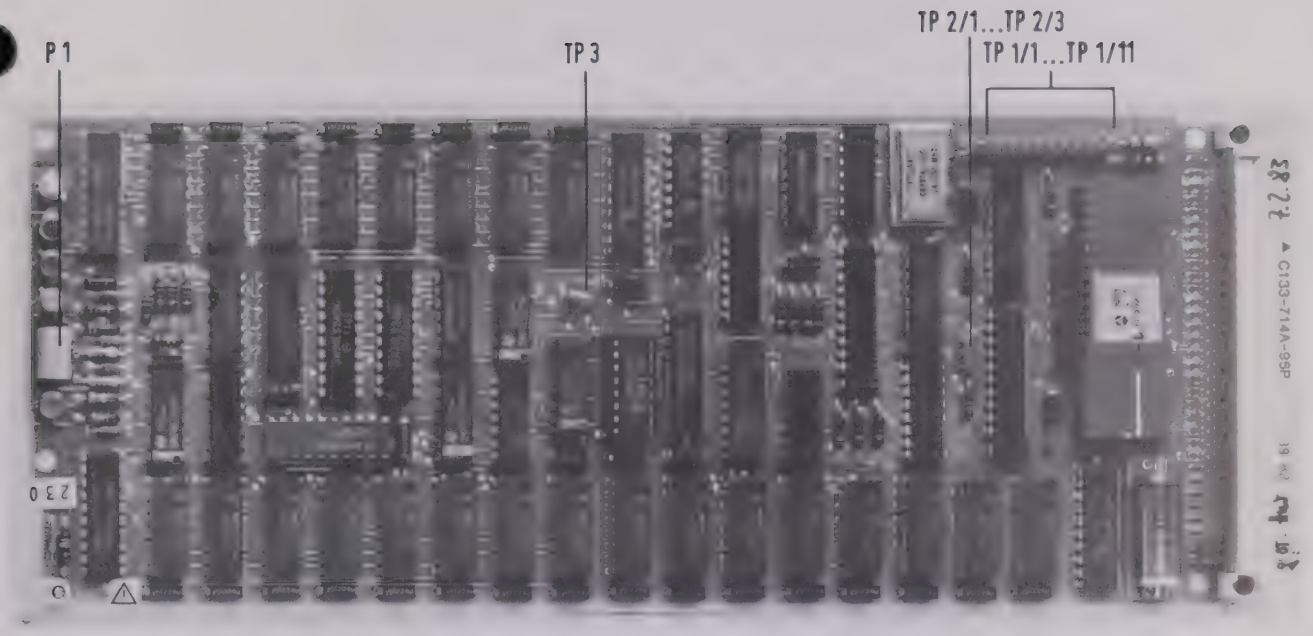


Figure 7-9 CRT control card (92) BN 962

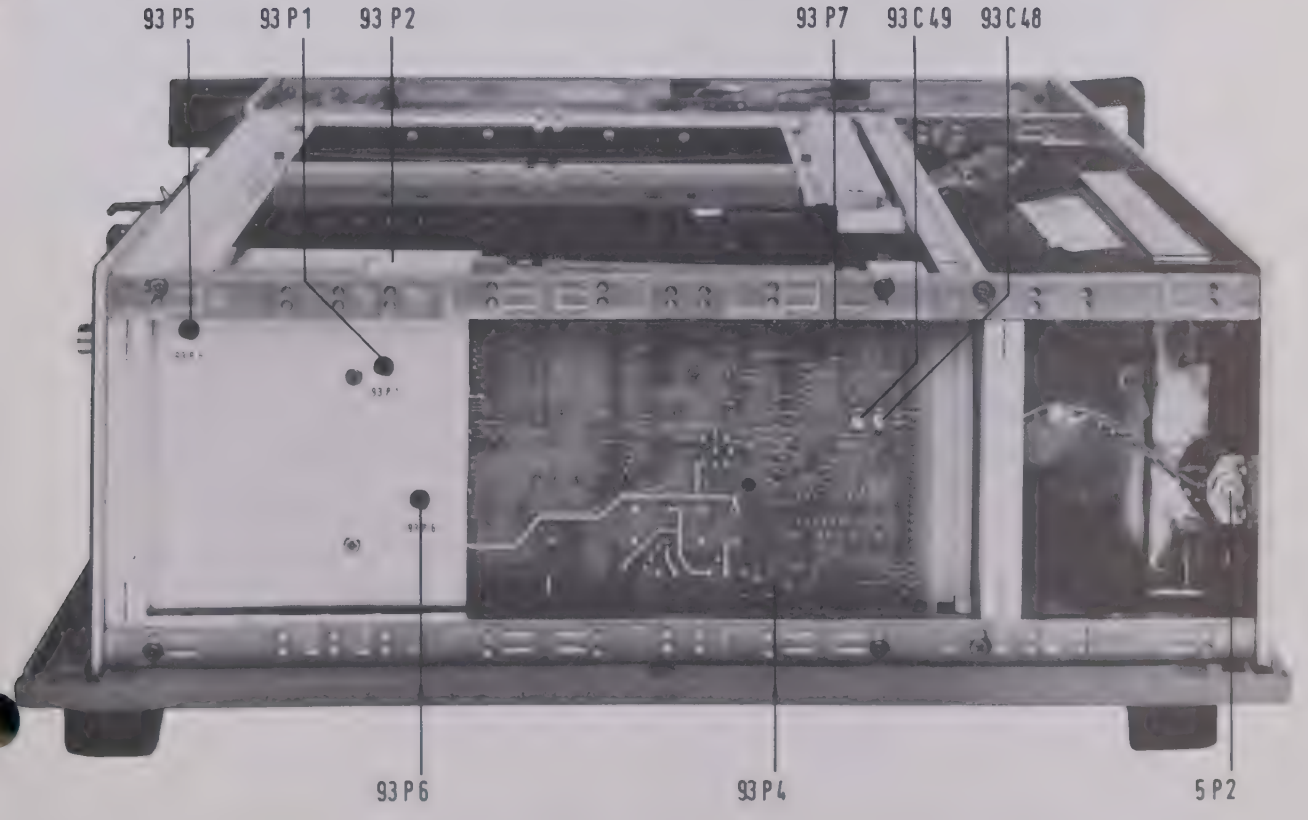


Figure 7-10 7" monitor (93) BN 980 in the SG-4

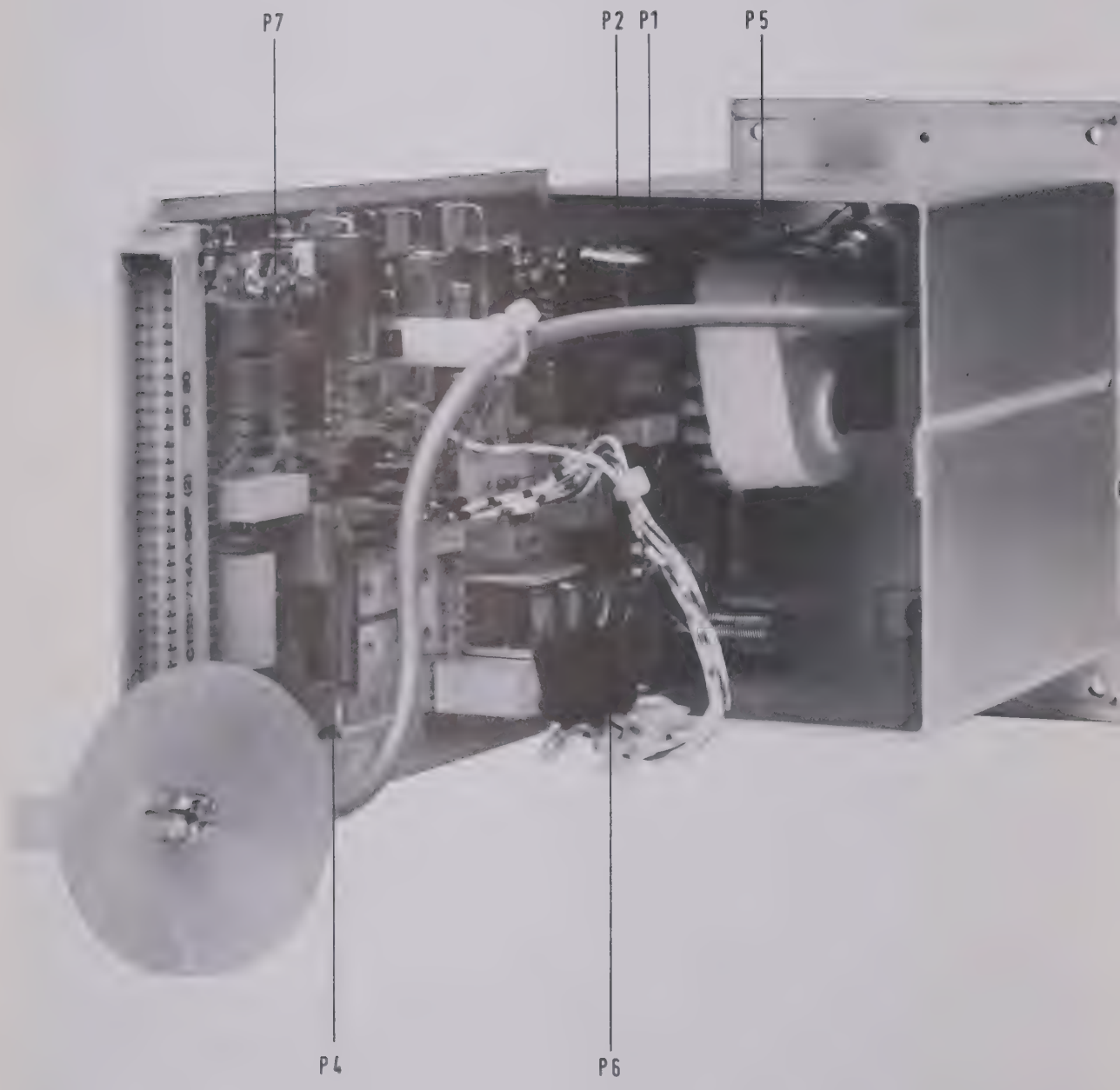


Figure 7-11 7" monitor (93) BN 980

7.3 TROUBLESHOOTING NOTES

7.3.1 CLEAR FUNCTION

When the power supply has been removed, the battery terminals taken off etc., the microprocessor must once more be brought to a well-defined output state. Meaningful data must also be written to the RAM. The SG-4 has the following facilities to carry out these procedures.

During the write procedure the microprocessor is reset by pressing LOCAL [20].

The instruction CLEAR 7xy* transferred via the IEC 625 bus also sets the microprocessor to the starting address zero. CLEAR can also be produced without the use of software by shorting together two contact areas on the CPU board after the covering plate has been removed.

In each case the program counter is set to zero and the processor restarts its initialisation routine. If the service switch or the free-run switch are not altered, the normal instrument software is run.

7.3.2 FAULT LOCALISATION PROCEDURE

The SG-4 has the following software troubleshooting aids:

- Automatic RAM/ROM test
- Automatic I/O test (high impedance test)
- Automatic testing of the digital section of the buffer and converter board
- Monitor program via IEC bus
- Stimulus programs for signature analysis CPU-II, buffer and converter board
- "Test card" for functional testing and setting the video control card and the monitor board with deflection unit
- Cyclic test for digital section of the buffer and converter board
- Program for testing the LEDs on the front panel
- Program for testing the key board
- Programs for adjusting the converter board

---

* Instrument address

7.3.3 AUTOMATIC TEST

After being switched on or after initiation of the clear function, the SG-4 performs an automatic test in the normal operating mode (service switch on processor card: 0).

If an error is detected the test is interrupted, the "Remote" and "Local" LEDs [6] flash alternately at 0.8 Hz, the SOD output of the processor emits a signal of the same frequency, and an error message is issued to the screen:

Error message	Test failed	Faultfinding reference
0030	ROM test	7.4.1
01FF	RAM test	7.4.2
02FF	IO test	7.4.3
0421	Clear buffer memory	7.4.5
0422	Buffer memory signature	7.4.6
0423	Inhibit buffer memory	7.4.7
0424	Convertor card/sweep counter	7.4.8
0425	Set buffer memory address	7.4.9
0426	Buffer memory/current values	7.4.10

Figure 7-12 Error messages for the activation test

7.3.4 CALLING A TEST

A test is called by setting the service switches to the number specified in the test, and then switching on the SG-4 or initiating the clear function in accordance with Section 6.1.2.

Every test can also be called under the specified address via the hardware monitor or IEC Bus. For this purpose, the service switches must be set to 0. Example: the test "Clear buffer memory" of 7.4.5 can be called via the IEC bus command

S: 0103.

7.4 FAULTFINDING IN THE CONTROL SECTION/DIGITAL SECTION

A series of tests is provided which can be performed either with the CPU card alone or with the intermediate memory and convertor cards.

7.4.1 ROM TEST

Service switch: 04

The test computes the check sum of each EPROM and compares it to the value in EPROM Ø. If an error occurs, a signal with a frequency of 280 kHz is output at the SOD output and "E" is output to the screen/monitor display.

Error message OOEX signifies that ROM X exhibits an incorrect check sum.

In the event of an error, check the following:

- $\overline{\text{Reset In}}$ = LOW (start-up circuit)
- TRAP, HOLD = LOW
- CLOCK = 4 MHz
- READY = HIGH
- Address signatures of ROM/RAM in the free-running state
- Data signatures of the ROMs in the free-running state

For free-running, see 9.2.5.7 and 6.1.3.

The software-independent free-running signatures of the address lines are:

Start: ⌐ TP ROM Ø - 6
Stop: ⌐ as for Start
Clock: ⌐ TP $\overline{\text{OE}}$
Frame signature: P 254

AØ	5P33
A1	FA11
A2	3HUA
A3	12UO
A4	C7A5
A5	46HC
A6	65CA
A7	8AUC
A8	9241
A9	1U5P
A10	AAHU
A11	U665
A12	826P
A13, A14, A15	equal to Ø or frame signature, depending on 8 k selector signal chosen for Start/Stop

The software-dependent signatures of the ROM data must be examined in the same way. Observe the correct choice of Start/Stop frame.

7.4.2 RAM TEST

Service switch: Ø1

When the test has been called, functioning of the RAM area is continuously checked. If an error occurs, a signal with a frequency of 60 kHz is outputted at the SOD output. If there is no error, a signal with a frequency of 280 kHz appears.

In the event of an error, check the address signatures as in ROM test 7.4.1. The following also apply, immediately at the RAMs:

AØ	CF67
A1	2845
A2	HUAP
A3	UOA4
A4	55U1
A5	A48U
A6	87PP
A7	68AU
A8	7015
A9	UHOA
A10	488C

7.4.3 IO TEST

Service switch: Ø3

When the test has been called, the IO strobe signals $\overline{RD}$', $\overline{WR}$', $\overline{LSS}$ are inhibited (HIGH) so that a connected peripheral device cannot interfere with the test. Various patterns are then selected on the IO data bus and read in again, so that any short circuit of the IO data lines IODØ-7 can be detected.

Refer to 9.2.5.8.

In the event of an error, a signal with a frequency of 280 kHz is output at the SOD output; otherwise 17 Hz.

For faultfinding, check the (M) signatures. Refer to 7.4.14.

Service switch: Ø2

After the call, the IO strobe signals $\overline{RD}$', $\overline{WR}$', $\overline{LSS}$ are enabled and the same addresses are called as above. Only output commands are generated without checking the function. The test is suitable for faultfinding with an oscilloscope.

7.4.4 TEST MODE OF THE CONVERTOR AND BUFFER MEMORY CARDS

The digital sections of both cards can be extensively checked by a test mode which can be activated. The following relationships apply:

X-addresses, Y-data, address change, BA, U/$\overline{D}$ (x), sweep out/$\overline{return}$, erase check byte

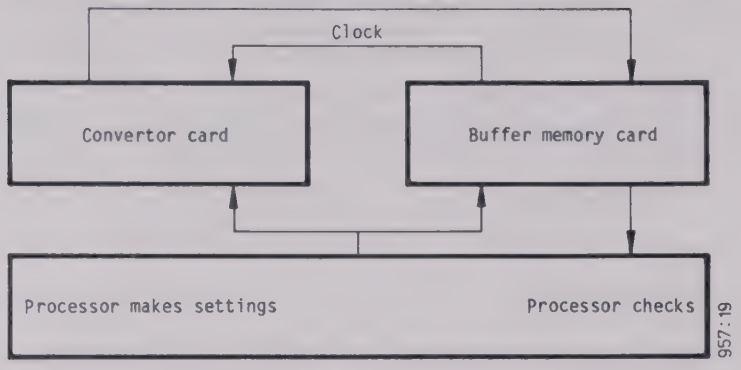


Figure 7-13 Test mode

Refer to Section 9.2.3.1: Range switching and test function

7.4.5 CLEARING THE BUFFER MEMORY

Service switch: 21 Address: 0103_H

This test affects the buffer memory and the convertor card. The processor makes the following settings:

8 → $1A_H$ (sweep out/return check): BA HIGH
$ØB_H$ → 14_H (mode control): test mode, off, signals from the convertor card are thus static
0 → $2C_H$, $2D_H$: set address counter to zero
1 → $2F_H$: enable memory
X → $2E_H$: clear memory

The processor checks the buffer memory for zero:

24_H check byte, bit Ø - 2
25_H minimum
26_H maximum
} 512 x 3 addresses

The following appears on the screen:

TE21 XXXX where the number of runs is XXXX
TE21 XXXX ER additionally appears in the event of an error and remains with a temporary error.

Faultfinding instructions:

Check (G) signatures of RD Ø-7 at buffer memory, R 22 and at read-gates for a check byte, minimum, maximum;
Examine (K) signatures RA Ø-10 and WE, OE at buffer memory;
Check resettability of the address counter by means of the monitor;
Check up-counting of addresses RA Ø-7 at RAM during the clearing command at the RAM (oscilloscope);
Check (H) frame signature (check of functional chain FF 24/2 set = read check byte, address counter counts another 4 addresses, FF 24/2 reset by decoder IC 4/2).
Check (H) signatures RA Ø-10 and WE, OE at the RAM;
Check (H) signatures at read-gates for check byte, minimum, maximum (only clock inputs).

7.4.6 BUFFER MEMORY SIGNATURE

Service switch: 22 Address: 0106_H

The convertor card is switched to test mode and the buffer memory is cleared. After t > 0.5 s the buffer memory is partially loaded with a data pattern. The processor checks the signature whilst reading out the buffer memory (check byte bits Ø-2, minimum, maximum).

The processor makes the following settings:

1 ⟶ $2F_H$ emory enabled
8 ⟶ $1A_H$ set sweep out/return check
3 ⟶ 14_H test mode on
0 ⟶ 10_H X-offset
OFF_H ⟶ 11_H X-amplification
0 ⟶ $2C_H$, $2D_H$ set address counter to zero
X ⟶ $2E_H$ clear buffer memory
0 ⟶ $2C_H$, $2D_H$ set address counter to zero
OF_H ⟶ $1A_H$ set sweep out/return check
1 ⟶ $2F_H$ enable memory.

After 0.5 s, reading out takes place with a signature check.

The following appears on the screen:

TE22 XXXX with number XXXX of test runs,
TE22 XXXX ER corresponding to the error event; remains displayed whilst the error disappears.

(re signature test)
Faultfinding instructions:

Check (K) signatures at buffer memory/convertor card interface (XA 3-11, Y Ø-7, BA, U/$\overline{D}$(x), sweep out/$\overline{return}$); if these agree, an error on the buffer memory card is probable; see Figure 7-13 (in Section 7.4.4).

Checking the convertor card:
Check (K) signatures of the convertor card
Check (M) signatures of the convertor card

Checking the buffer memory card:
Check the signatures as for faultfinding in Section 7.4.5. If the (G) signatures are faulty:
Check (K) signatures;
Check (J) signatures;
Check (O), (P) and (Q) signatures;
Check (R') to (T) signatures.

7.4.7 INHIBITING THE BUFFER MEMORY

Service switch: 23 Address: 0109_H

The processor calls the previous test, which causes the buffer memory to be loaded with the data of a specified signature.

It then inhibits and clears the memory:

$0 \rightarrow 2C_H$, $2D_H$	set address counter
$0 \rightarrow 2F_H$	inhibit memory
$0 \rightarrow 2E_H$	clear memory

It now compares the signature as in the previous test. The clear instruction must not have become effective.

The following appears on the screen:

TE23 XXXX	with number XXXX of runs
	or
TE23 XXXX ER	corresponding to the error

Faultfinding: check (M) signatures on buffer memory IC 17; (J) signatures at IC 18.

7.4.8 SWEEP COUNTER

Service switch: 24 Address: $010C_H$

This test only affects the convertor card.
Firstly, test mode is switched off and on

$ØB_H \rightarrow 14_H$

and the current status of the sweep counter (address $1B_H$) is loaded into an RAM.

By means of the cycle

$Ø3_H \rightarrow 14_H$ test mode on

wait 0.21 sec

$ØB_H \rightarrow 14_H$ test mode off

the sweep counter can be made to count up (narrow pulse at the PEN DOWN simulation IC 13.1.2; T 0.21 s) and compared with the internal memory which has counted up. All 16 counter settings are checked.

The following appears on the screen:

TE24 XXXX	with number XXXX of runs
	or
TE24 XXXX ER	corresponding to the error event

Faultfinding: (K) signatures at sweep out/return check, (M) signatures at IC 20, examination of periodic counter signals at IC 24 with an oscilloscope.

7.4.9 SET ADDRESS COUNTER

Service switch: 25 Address: $010F_H$

The buffer memory signature test must previously be called (service switch 22), so that the buffer memory is loaded with test data.

Various values are selected at address counter IC 32, 33, 34 (buffer memory) and the corresponding data - check byte, minimum, maximum - are checked.

The following appears on the screen:

TE25 XXXX	with number XXXX of runs
	or
TE25 XXXX ER	corresponding to the error event

For faultfinding: perform previous tests and check the settability of the address counter by means of the monitor.

7.4.10 CURRENT VALUES

Service switch: 26 Address: 0112_H

The buffer memory and convertor cards are switched to test mode, as in the signature test of 7.4.5. Certain combinations of current values thus occur periodically. The following are checked:

Current value 1	Current value 2	Current value 3	must appear
28_H	29_H (bits 5-7)	$2A_H$	at the latest after
(XLSB)	(check byte)	(Y)	
33_H	$C0_H$	FF_H	0.4 s
00_H	00_H	00_H	0.23 s
33_H	$C0_H$	FF_H	0.17 s

The following appears on the screen:

TE26 XXX with number XXXX of runs
or
TE26 XXXX ER corresponding to the error event

For faultfinding: check the (M) and (K) signatures at the output gates for the current values.

7.4.11 READY - CURRENT VALUES

Service switch: 33 Address: 0127_H

The processor successively reads in the current value "1 28_H". Loading of the output gates - current value/1/2/3; 28_H, 29_H, $2A_H$ - can be checked in accordance with Figure 9-13 using an oscilloscope.

7.4.12 READY - CHECK BYTE

Service switch: 34 Address: $012A_H$

The processor successively reads check byte 24_H.
Loading of the output gates - check byte 24_H, minimum 25_H and maximum 26_H - can be checked in accordance with Figure 9-14 using an oscilloscope.

7.4.13 READY - CLEAR MEMORY

Service switch: 35 Address: $012D_H$

The processor continuously processes the following program:

$OFF_H \rightarrow 2D_H$, $2C_H$ address counter at address 511
$OFF_H \rightarrow 2E_H$ clear memory, only highest 4 addresses

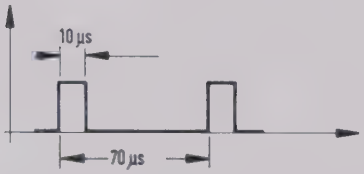


Figure 7-14 Signal at 4 IC 27.1

7.4.14 SIGNATURE LISTS

The signature of a line can be found under the designation of the corresponding input or under the name used for the line in the circuit diagram.

The signatures are examined with the hp 5004 A signature analyzer. All signatures are also listed according to lines or ICs in Section 7.4.15.

(H) signatures of the buffer memory card [957-A] circuit diagram (4)

Clock: ⌐ 31.3
Start: } S0D,
Stop: ⌙
Service switch:22

Frame signature:	A70U	memory control
ZAØ	62UA	
ZA1	21A9	
4 IC 26.4	P0P8	
4 IC 41.11	04F4	maximum input gate
4 IC 40.11	8262	minimum input gate
4 IC 39.11	F131	kbyte input gate
4 IC 28.4	F131	
4 IC 30.13	4797	RAM enable logic
4 IC 42.2.4.5	P098	
4 IC 38.21	4797	RAM
4 IC 38.20	P098	
ZAØ, RAØ	62UA	addresses, address counter,
ZA1, RA1	21A9	changeover switch, buffer memory
ZA2, RA2	A077	
ZA3, RA3	0AAH	
ZA4, RA4	0309	
ZA5, RA5	442A	

Continued on Page 7-24

ZA6, RA6	U2A7	
ZA7, RA7	7722	
ZA8, RA8	6358	
ZA9, RA9	7349	
ZA10, RA10	P54P	
ZA11 -	000U	
RDØ	1PFH	RAM data
RD1	0U3A	
RD2	322F	
RD3	H954	
RD4	600F	
RD5	3561	
RD6	7662	
RD7	46FF	

re (H) signatures

Note:
If errors have occurred so far, they must be discovered by means of an oscilloscope. Only continue when the errors have been eliminated.

(J) signatures of buffer memory card [937-A] circuit diagram (4)

Clock: ⌐└ Ta 400/2
Start: ⌐└ } U/$\overline{D}$(x)
Stop: └⌐ }
Service switch:22

Frame signature:	H57U	
M/Ø	574A	minimum value formation
M/1	92H6	
M/2	999Ø	
M/3	H4P6	
M/4	AH24	
M/5	448H	
M/6	5852	
M/7	3P9H	
4 IC 17.5	2F73	
4 IC 17.6	A3A7	
4 IC 16.1	8526	
4 IC 16.2	CAFØ	
4 IC 16.8	0F6U	
4 IC 6.1	31F4	

Continued on Page 7-25

4 IC 17.1	O11P	maximum value formation
4 IC 17.2	1414	
4 IC 16.11	C69H	
4 IC 16.12	866H	
4 IC 16.13	8526	
4 IC 6.6	995O	
MAØ	84F2	
MA1	F1C6	
MA2	41C3	
MA3	5FCA	
MA4	O3C7	
MA5	H32U	
MA6	4659	
MA7	956C	
4 IC 19.1	OC75	resetting of min/max formation
4 IC 16.3	OC75	by address change
4 IC 16.4	19CU	
4 IC 16.5	4293	
4 IC 3.13	19CU	transfer of min/max
4 IC 3.14	4293	values by address change
4 IC 3.15	4UO8	
4 IC 18.2	HIGH	
4 IC 18.5	3FCO	
4 IC 21.1	88HP	
4 IC 22.1	7CAU	
4 IC 23.1	CF79	

re (J) signatures

Note: in the event of an error in the minimum-maximum value formation, open the feedback path and apply logic LOW to 4 IC 6.1.6. The following then apply:

M/Ø, MAØ	55U4
M/1, MA1	229C
M/2, MA2	72U7
M/3, MA3	186H
M/4, MA4	H6A2
M/5, MA5	7PH8
M/6, MA6	OUO7
M/7, MA7	7614
4 IC 17.1	AP98
4 IC 17.2	F343
4 IC 17.5	3H5U
4 IC 17.6	AP98
4 IC 16.1	8226
4 IC 16.2	4065
4 IC 16.8	O6HH
4 IC 16.11	8326
4 IC 16.12	3C82
4 IC 16.13	8526

(K) signatures:

Clock: ⌐ Ta 400/2
Start: ¬ } U/$\overline{D}$(X)
Stop: ¬ ┘
Service switch: 22

Frame signature:	H57U	
XA3, RA2	PHHP	X-addresses (buffer memory/convertor card)
XA4, RA3	1P97	X at = at (buffer memory), RAM
XA5, RA4	HUPF	addresses (buffer memory)
XA6, RA5	U930	
XA7, RA6	HPHA	
XA8, RA7	24P8	
XA9, RA8	41HF	
XA10, RA9	6H76	
XA11, RA10	UU9P	
4 IC 30.12	4U08	RAM enable logic (buffer memory)
4 IC 35-37.9	65AP	address separator (buffer memory)
4 IC 35-37.14	C0H1	
YØ	ACP8	interface (buffer memory/convertor card)
Y1	3AC6	
Y2	P5PU	
Y3	4U5A	
Y4	AH45	
Y5	UHC0	
Y6	1P0P	
Y7	PF28	
BA	PU97	
U/$\overline{D}$(x)	2300	
Sweep out/return	H736	
Address change	HP0A	
Erase check byte	LOW	
3 IC 33.12	045H	mode control (convertor card)
3 IC 4.9	180C	
3 IC 1.5	180C	Y-convertor (convertor card)
3 IC 9-10.1	180C	
3 IC 9-10.7	56F7	
3 IC 10.15	83C8	
3 IC 33.2	474C	changeover switch X-channel (convertor card)
3 IC 13.9	H1PF	
3 IC 13.10	LOW	
3 IC 3.10	0493	X-convertor (convertor card)
3 IC 14.9	0493	
3 IC 17.9	4601	
3 IC 19.21, 23.9	474C	counter X-convertor

3 IC 35.12	LOW	
3 IC 25.3	AF9O	
3 IC 19.21, 23.15	92U3	
3 IC 26.5	2149	
3 IC 26.6	HIGH	
3 IC 25.4	HIGH	
3 IC 31.5	H1PF	
3 IC 22.9.10 11	HIGH	sweep out/return check (convertor card)
3 IC 18.12. 15.19	LOW	
3 IC 22.13	H736	
3 IC 29.8	PHHP	
AØ	AF8F	address change detection,
A1	H61U	hysteresis x-convertor (convertor card)
A2	63U5	
3 IC 29.5	755P	
3 IC 29.6	FFCA	
3 IC 30.1.5	6F9C	
3 IC 30.2.9. 11.13	LOW	
3 IC 30.3	92U3	

The (K) signatures can also be measured in test mode, service switch: 31. Any errors caused by nested buffer memory writes/reads can result from the fact that the memory is only loaded there, but the processor has been stopped.

(M) signatures

Clock: ⌐¬ $\overline{LSS}$
Start: ⌐ } SOD
Stop: ¬⌐
Service switch:30

The processor writes data into all output gates of the buffer memory and convertor card, so that each output line (and IODØ-7 and some gate-selector lines) have their own signatures. No meaningful mode is selected.

Frame signature:	72A2	
IOAØ	7A06	IO addresses
IOA1	PIPO	
IOA2	7H47	
IOA3	9878	
IOA4	P733	
IOA5	9591	
IOA6	LOW	
IOA7	LOW	
4 IC 2.1	P733	IO address decoding (buffer memory)
4 IC 4.1	P733	
4 IC 32, 33.1	PU91	address counter (buffer memory)
4 IC 34.1	940A	
4 IC 26.11	LOW	clear memory (buffer memory)
4 IC 43.3	PPOA	inhibit memory (buffer memory)
4 IC 25.13	0010	check byte (buffer memory)
IODØ	C56F	IO data
IOD1	084P	
IOD2	8423	
IOD3	56CU	
IOD4	AC5C	
IOD5	H5A9	
IOD6	2075	
IOD7	103P	
3 IC 4.10	052A	Y-changeover switch (convertor card)
3 IC 4.11	0A55	
3 IC 13.10	0295	X-changeover switch (convertor card)
3 IC 34.11	814A	binary counter (convertor card)
c3	0010	delite check byte
3 IC 35.4	0020	sweep out/return check (convertor card)
3 IC 22.9	0102	
3 IC 22.10	0205	
3 IC 22.11	040A	
3 IC 31.9	0081	
3 IC 27.5	0040	address change detection (convertor card)
3 IC 30.2	0040	
3 IC 39.15	9591	IO address decoding (convertor card)
3 IC 38.1	72AP	

3 IC 38.15	9A74	
3 IC 39.1	7H4C	
3 IC 18.11	P733	
3 IC 28.2.3. 4.5	72A3	
3 IC 25.11.12. 13	72AO	
3 IC 32.9	9A76	
3 IC 16.13	72A6	
3 IC 12.13	72AA	
3 IC 37.4	0001	interrupt check (convertor card)
3 IC 37.10	0002	

(O) signatures of the buffer memory card [957-A] circuit diagram (4)

Serves for decoding whether, in the event of incorrect RAM data RDØ-7, the cause is FF IC 21.

Clock: IC 21.1
Start: } U/$\overline{D}$(x)
Stop: }
Service switch:31

Frame signature:	PFHO
RDØ	H492
RD1	58FC
RD2	5FA9
RD3	4279
RD4	C2F6
RD5	CUU7
RD6	H52U
RD7	993U

(P) signatures

as for (O) signatures in regard to FF IC 22,
Clock: IC 22.1

Frame signature:	PFHO
RDØ	U28F
RD1	P5CO
RD2	FHAP
RD3	U848
RD4	U951
RD5	P03C
RD6	HP82
RD7	521H

(Q) signatures

as for (0) signatures in regard to FF IC 23,
Clock: IC 23.1

Frame signature:	PFHO
RDØ	U91C
RD1	UHC8
RD2	04A3
RD3	LOW
RD4	LOW
RD5	LOW
RD6	LOW
RD7	LOW

(R') signatures of the buffer memory card [957-A] circuit diagram (4)

Checking the check byte of the output gate, input data
Clock: ⌐ IC 39.11
Start: ⌐ } SOD
Stop: ⌐ }
Service switch:22

Frame signature:	4596
RDØ	C6UO
RD1	A6AU
RD2	1O5U
RD3	OOOO

(R) signatures of the buffer memory card [957-A] circuit diagram (4)

Checking the output gate minimum, input data
Clock: ⌐ IC 39.1
Start: ⌐ }
Stop: ⌐ } SOD
Service switch:22

Frame signature:	4596
IODØ	C6UO
IOD1	A6AU
IOD2	1O5U
IOD3	OOOO

(S') signatures of the buffer memory card [957-A] circuit diagram (4)

Checking the output gate minimum, output data

Clock: ⌐ IC 40.11
Start: ¬ ⌋
Stop: ⌐ } SOD
Service switch:22

Frame signature:	4596
RDØ	AAUU
RD1	7605
RD2	A1U5
RD3	6CH5
RD4	H084
RD5	9H18
RD6	CPC4
RD7	FA03

(S) signatures

Checking the output gate minimum, input data.

Clock: ⌐ IC 40.1
Start: ¬ ⌋
Stop: ⌐ } SOD
Service switch:22

Frame signature:	4596
IODØ	AAUU
IOD1	7605
IOD2	A1U5
IOD3	6CH5
IOD4	H084
IOD5	9H18
IOD6	CPC4
IOD7	FA03

(T) signatures of the buffer memory card [957-A] circuit diagram (4)

Checking the output gate maximum, input data

Clock: ⌜ IC 41.11
Start: ⌞ } SOD
Stop: ⌜ }

Service switch:22

Frame signature:	4596
RDØ	HAH7
RD1	FCCP
RD2	2195
RD3	P832
RD4	360A
RD5	OHH3
RD6	C545
RD7	7638

(T) signatures

Checking the output gate maximum, output data

Clock: ⌜ IC 41.1
Start: ⌞ } SOD
Stop: ⌜ }

Service switch:22

Frame signature:	4596
IODØ	HAH7
IOD1	FCCP
IOD2	2195
IOD3	P832
IOD4	360A
IOD5	OHH3
IOD6	C545
IOD7	7638

(Y) signatures of the buffer memory card [957-A] circuit diagram (4)

Checking the operation to delete the highest buffer memory address.

Clock: ⌞ Ta 400/2
Start: ⌜ } IC 27.1
Stop: ⌞ }

Service switch:35

Frame signature:	000U
ZAØ	0005
ZA1	0003
ZA11	0000
4 IC 42.1.10	000P

7.4.15 CROSS-REFERENCE FOR SIGNATURE LIST

For the signatures specified in Section 7.4.14, the following list applies in order to find the signature names for a line to be checked on the buffer memory or convertor card, or the IO bus of the entire SG-4. Lines not indicated must be checked in another way.

The signature of a line can be found under the designation of the corresponding input or under the name used in the circuit diagram.

There is a signature for the following lines which are provided with names:

Address change	K
A0-2	K
BA	K
Sweep out/return check	K
IOA0-7	M
IOD0-7	M, R, S, T
Erase check byte	K, M
MA0-7	J, J
MI0-7	J, J
RA0, 1	H
RA2-10	H, K
RD0-7	H, O, P, Q, S', T'
RD0-3	R'
U/$\overline{D}$(X)	K
XA3-11	K
Y0-7	K
ZA0, 1	H, Y
ZA2-10	H
ZA11	H, Y

There is a signature for the following IC connections (only affects buffer memory card (4) [957-A] and convertor card (3) [957-B]):

3 IC 1.5	K
3 IC 3.10	K
3 IC 4.9	K
3 IC 4.10. 11	M
3 IC 9.1. 7	K
3 IC 10.1 7. 15	K
3 IC 12.13	M
3 IC 13.9	K
3 IC 13.10	K, M
3 IC 14.9	K
3 IC 17.9	K
3 IC 16.13	M
3 IC 18.12 15. 19	K
3 IC 18.11	M
3 IC 19.9. 15	K
3 IC 21.9. 15	K

3 IC 22.9. 10. 11	K, M
3 IC 22.13	K
3 IC 23.9. 15	K
3 IC 25.3. 4	K
3 IC 25.11. 12. 13	M
3 IC 26.5. 6	K
3 IC 27.5	M
3 IC 28.2. 3. 4. 5	M
3 IC 29.5. 6. 8	K
3 IC 30.1.3.5.9.11.13	K
3 IC 30.2	K, M
3 IC 31.5	K
3 IC 31.9	M
3 IC 32.9	M
3 IC 33.2. 12	K
3 IC 34.11	M
3 IC 35.4	M
3 IC 35.12	K
3 IC 37.4. 10	M
3 IC 38.1. 15	M
3 IC 39.1. 15	M
4 IC 2.1	M
4 IC 4.1	M
4 IC 3.13. 14. 15	J
4 IC 6.1, 6	J
4 IC 16.1.2.3.4.5.8.11.12.13	J, J
4 IC 17.1. 2. 5. 6	J, J
4 IC 18.2. 5	J
4 IC 19.1	J
4 IC 21.1	J
4 IC 22.1	J
4 IC 23.1	J
4 IC 25.13	M
4 IC 26.4	H
4 IC 26.11	M
4 IC 28.4	H
4 IC 30.12	K
4 IC 30.13	H
4 IC 32.1	M
4 IC 33.1	M
4 IC 34.1	M
4 IC 35.9. 14	K
4 IC 36.9. 14	K
4 IC 37.9. 14	K
4 IC 38.20. 21	H
4 IC 39.11	H
4 IC 40.11	H
4 IC 41.11	H
4 IC 42.1. 10	Y
4 IC 42.2. 4. 5	H
4 IC 43.3	M

7.4.16 CONTINUOUS TEST

Service switch: 20 Address: 0100_H

Tests 7.4.5 to 7.4.11 are run through cyclically.

The following appears on the screen:

DT2X NNNN with selection NNNN of runs
or
DT2X NNNN YY in the event of an error.
The display is maintained.
The following table applies to YY.

YY	test failed
21	7.4.5 clear buffer memory
22	7.4.6 buffer memory signature
23	7.4.7 inhibit buffer memory
24	7.4.8 sweep counter
25	7.4.9 set address counter
26	7.4.10 current values

7.5 FAULTFINDING IN THE ANALOG SECTION (3)

7.5.1 Y-CHANNEL

Freedom from faults in the digital section by means of switch on test or continuous test.

Use the setup of the alignment instructions of Section 7.7.2.

The following tables contain a series of voltages as encountered in the analog section. Additionally, digital output value of the A/D convertor is represented in averaged form.

Tolerances: $V \leq 0.1$ V: $\pm$ 15 mV
$0.1 \text{ V} < V \leq 1$ V: $\pm$ 25 mV
$V > 1$ V: $\pm$ 60 mV

7.5.1.1 2 dB logarithmizer

Service switch: 37 Address: 0133_H

At 3TP2 check for V_{ref+} = +8.0 V and at 3TP3 check for V_{ref-} = -8.0 V.

Y-input voltage from PSU	IC 4.15 IC 1.5	TP 1 IC 1.7	Reading: Digital value
36 mV	29 mV	47 mV	007 ... 019
3.97 V	2.95 V	4.72 V	957 ... 969
0.40 V	0.32 V	0.52 V	0E7 ... 129
2.02 V	1.57 V	2.51 V	4E7 ... 519
3.24 V	2.45 V	3.92 V	7B7 ... 7E9
4.99 V	3.62 V	5.8 V	B77 ... BB9
6.36 V	4.5 V	7.2 V	E47 ... E79

Figure 7-15 Voltages at the 2 dB logarithmizer

7.5.1.2 80 dB path

Service switch: 39 Address: 0139_H

At TP 2 check for V_{ref+} = +8.0 V

Y-input voltage from PSU	IC 4.13 IC 1.5	TP 1 IC 1.7	Reading:
5.0 V	4.7 V	7.5 V	F07 ... F19

Figure 7-16 Voltages at the 80 dB path

7.5.1.3 20 dB logarithmizer

Service switch: 38 Address: 0136_H

At TP 2 check for V_{ref+} = +8.0 V and at TP 3 check for V_{ref-} = 8.0 V.
IC 3.3: +4.0 V
T 2 emitter: +4.0 V

Y-input from PSU	IC 1.8	IC 2.3	IC 2.6	IC 4.14 IC 1.5	TP 1 IC 1.7	Reading
0.40 V	≈ -2.4 V	60 mV	3.9 V	29 mV	47 mV	007 ... 019
3.975 V	≈ -4.0 V	≈ 0 (30µV)	2.1 mV	3.93 V	6.29 V	C77 ... C89

Figure 7-17 Voltages at the 20 dB logarithmizer

For controlling the changeover switch IC 4 see Figure 9-5 of the circuit description: for functioning of the A/D convertor see also circuit description.

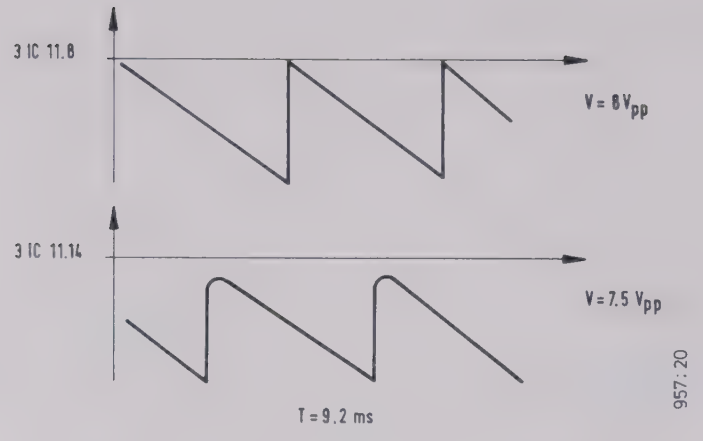
Alignment of the Y-channel is described in Section 7.7.2.

7.5.2 X-CHANNEL

7.5.2.1 Offset calibration and gain calibration

Service switch: 29 Address: $011B_H$

The two D/A convertors on convertor card IC 12, IC 16 are loaded cyclically with increasing values. Check the following with an oscilloscope:

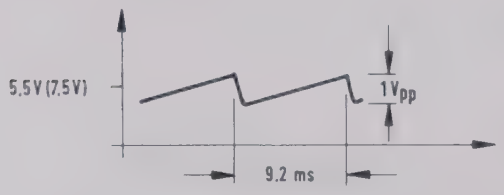


7.5.2.2 Lowpass filter, changeover switch

Service switch: 29 Address: $011B_H$

The X-input is switched through to the A/D convertor by changeover switch 3 IC 13. The offset and gain calibration are cyclically loaded as in 7.5.2.1. It is thus possible to check the extent to which the input voltage of the X-convertor 3 IC 15.16 is shifted by the d.c. component at an X-input voltage at socket [20]:

A voltage of 0 V (2 V) should be applied to 3 Bu 1 [20].
Check: 3 IC 3.10: 0 V (2 V)
3 IC 15.16:



The cutoff frequency of the lowpass filter is 600 Hz.

Faultfinding: (K) signatures at X-addresses XA 3-11.

7.7 ALIGNMENT INSTRUCTIONS

7.7.1 SUMMARY

Trimmer	Alignment
3 P 1	Offset 1/20 dB logarithmizer
3 P 2	Offset 2/20 dB logarithmizer
3 P 3	Gain 20 dB logarithmizer
3 P 4	Gain 80 dB path
3 P 5	Gain 2 dB logarithmizer
3 P 6	Offset 2 dB logarithmizer
3 P 7	Reference voltage +8 V

Figure 7-18 List of all alignment elements

7.7.2 ALIGNMENT OF THE Y-CHANNEL (3 P 1 ... 3 P 7)

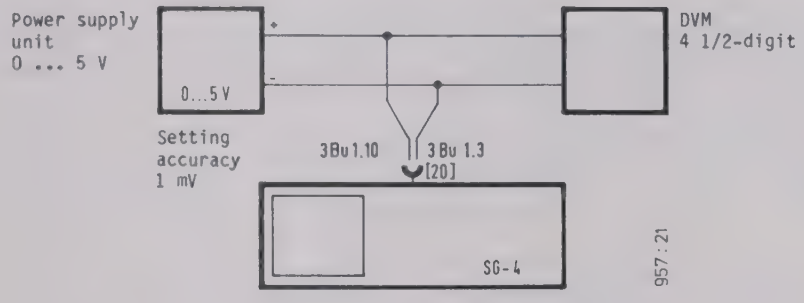


Figure 7-19 Alignment setup

After setting of the service switch as specified and after initiating the clear function, the Y-voltage is displayed digitally.

Reference voltage +8.0 V (3 P 7)

Connect digital voltmeter to 3 TP 2 (convertor card); ground remains at pin 3 of the Amphenol socket. Set 3 P 7 for +8.000 V $\pm$ 1 mV.

2 dB logarithmizer (3 P 5, 3 P 6)

Service switch: 37 Address: 0133_H

Power supply unit: set voltage to 36 mV.

Set 3 P 6 so that
Y -2 dB: 0010
is displayed.

Power supply unit: voltage at 3.966 V ± 1 mV
Set 3 P 5 so that
Y -2 dB: 0960
is displayed.

Repeat the alignment twice; any lack of accuracy in the display is then within the tolerance limits.

Alignment of the 2 dB logarithmizer affects the accuracy of the 20 dB logarithmizer and of the 80 dB path.

80 dB path (3 P 4)

Service switch: 39 Address: 0139_H

Power supply unit: set voltage to 4.985 V ± 1 mV. Set 3 P 4 so that
Y -80 dB: 0F00
is displayed.

20 dB logarithmizer (3 P 1, 3 P 2, 3 P 3)

Service switch: 38 Address: 0136_H

Power supply unit: set 0.402 V ± 1 mV.
Set 3 P 1 so that the voltage across resistor 3 R 15 or between TP 6 and TP 7 (Series C...) is equal to the output voltage of the power supply unit.

Power supply unit: set voltage to 0.402 V ± 1 mV.

Set 3 P 2 so that
Y -20 dB: 0010
is displayed.

Power supply unit: set voltage to 3.975 V ± 1 mV.

Set 3 P 3 so that
Y -20 dB: 0C80
is displayed.

Repeat the alignment twice; any lack of accuracy in the display is then within the tolerance limits.

7.8 FAULTFINDING ON BSK 1 BN 962 circuit diagram (92)

Call the test image as in 7.11.1; check the video signal at 93 Bu 1 at the rear of the unit: V_{pp} ~1 V.
Check the (M) signatures from Section 7.4.14.

7.9 FAULTFINDING ON THE IEC BUS CARD BN 958 circuit diagram (91)

7.9.1 PRELIMINARY NOTE

A prerequisite to testing the IEC 625 interface card is that the digital functions of the SG-4 in regard to program execution and driving of the SG-4 interface for the IEC 625 interface card operate perfectly.

The functions of the IEC 625 interface card can then be checked by means of a GO/NOGO test, during which the SG-4 is driven by an HP 85 desk computer (as IEC 625 bus controller).

In the event of an error, the IEC 625 interface card must be replaced.

7.9.2 CARD MARKINGS

The series index of the interface card is printed on an adhesive label on the IEC 625 interface card; e.g. A- ... for A-Series.

7.9.3 GO/NOGO TEST WITH HP 85 DESK COMPUTER

Test programs IECBT1 and IECBT2 are required for the GO/NOGO test with the HP 85 desk computer.

The test sequence utilizes an interactive dialog between the tester and the monitor screen. During the test, the special function keys k1 ... k4 (immediately below the screen) are used for stepping through the program, when the settings or tests requested on the screen have been performed or when an automatically running program section has been terminated. The functions of the special function keys are displayed on the screen immediately above the relevant keys.

For testing with IECBT1 and IECBT2, the normal SG-4 program must be activated on the SG-4 (i.e. no other test program may be present).

Test sequence:

Load test program IECBT1:	key "LOAD"	(Key in) "IECBT1"	key "END LINE"
Start test program IECBT1:	key "RUN"		

Perform the tests in accordance with the interactive dialog!
If "IECBT1 TERMINATED: TEST OK" is displayed,
continue the GO/NOGO test with test program IECBT2:

Load and start test program IECBT2:
Press special function key "CALL FROM IECBT2".

Perform the tests in accordance with the interactive dialog!
In event of error: do not troubleshoot, but replace
IEC 625 interface card!

Note:
Test program IECBT2 can also be loaded and started as follows:

Load test program IECBT2:	key "LOAD"	(Key in) "IECBT2"	key "END LINE"
Start test program IECBT2:	key "RUN"		

7.10 FAULTFINDING AT THE INPUT CIRCUIT (2)

7.10.1 LED TEST

When the test has been called, each LED of the entry circuit is switched on individually. Sequencing takes place after approximately 0.5 s. Inspect visually to ensure that all LEDs light up individually.

Troubleshoot using the oscilloscope and by testing the (M) signatures from 7.4.14.

7.10.2 KEYBOARD TEST

Service switch: 41 Address: $013F_H$

When the test has been called, the keyboard is read in at the 0.5 s rate. The result is displayed:

KEY: XX

The following apply:

Display XX	key
FF	no key pressed
03	soft key 1 (above)
00	soft key 2
05	soft key 3
01	soft key 4
04	soft key 5
02	soft key 6
08	scale menu
13	A
18	A-B
1B	A&B
20	B
14	hold
19	max. hold
1C	AVRG A
21	store A→B
28	←cursor pos
29	→cursor pos
2A	↓
2B	↑
2C	→fcent
2D	→REF.L.
38	LOCAL

A logic high on interrupt line RST 5.5 is indicated by

KEY: XX I.

After each scan and display of the keyboard, key interrupt 38_H and INT 1 interrupt 17_H are cleared on the convertor card. If the key interrupt via the convertor card reaches RST 5.5 of

the CPU, this "I" must appear exactly once per key stroke and must disappear with the next display (corresponds to RST 5.5 LOW).

Faultfinding using the oscilloscope: IO addresses and IO data can be checked by means of (M) signatures.

7.11 FAULTFINDING ON THE 7" MONITOR

7.11.1 CALLING THE TEST IMAGE

Service switch: 36 Address: 0130_H

When the SG-4 has been switched on, a test image is output by CPU-II to the CRT control card, circuit diagram (92) BSK-1. From there, the video signal is fed to the monitor card.

The individual signals can be followed in the circuit diagram.

8 CHECKING OF IMPORTANT TECHNICAL DATA

8.1 INTRODUCTION

Described in the following are procedures which allow the most important specifications of the unit to be checked. Where possible, standard commercial measuring equipment is proposed.

If no restriction is indicated, the tests should be made within the rated ranges of use of temperature and a.c. line voltage.

If a warm-up time is specified with the technical data, the tests should only be begun when this time has elapsed.

Checking of the most important data is intended to establish whether a measured variable displayed is within the guaranteed error limits. The check is only valid without reservations if the intrinsic errors of the measuring setup used are negligible.

Otherwise, the following rule applies:

If the error of the measuring setup used is $\pm$ m and if $\pm$ e is specified as guaranteed error limit for the specimen,

exceeding the limits $\pm$ (e + m)
demonstrates that the guaranteed error limits
will definitely be exceeded;

exceeding of the limits $\pm$ (e - m)
demonstrates that the guaranteed error limits
will definitely be respected.

The values for e and m are specified in each measuring specification. Value m is governed by the measuring instrument used and must therefore be respecified if the measuring specification is not complied with.
A systematic check of the data should follow the order specified here.

The test item should not be aligned until it is established that limit $\pm$ (e + m) has been exceeded.

8.2 ERROR CHARACTERISTICS OF THE SG-4

Measuring equipment required:

1 Selective Level Meter	SPM-19	BN 829	W & G
1 Level Generator	PS-19	BN 870	W & G
1 digital voltmeter	8600 A		Fluke

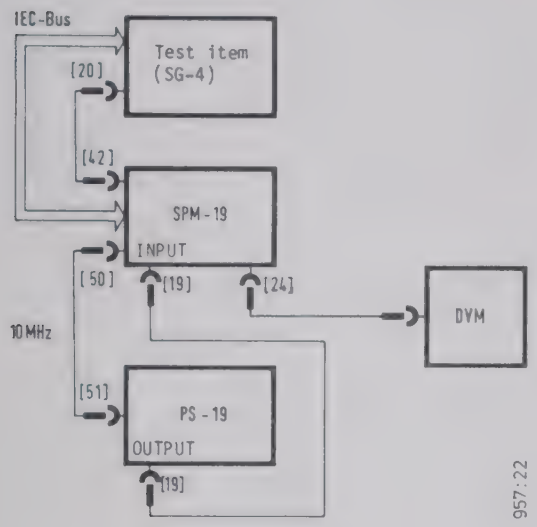


Figure 8-1 Measuring setup

Equipment settings:

SG-4:			
INTERFACE BUS IEC 625, address		:	1 less than that of the SPM-19
SC		:	ON
SCALE MENU	[2]	:	OFF
VIEW	[3]	:	A
PS-19:			
OUTPUT	[15]	:	Z = 75 Ω
Level	[2], [3], [4], [5]	:	0 dB/dBm
Frequency	[8], [13]	:	9 MHz

SPM-19:

DISPLAY	[3] :	ABS
MODE	[4] :	ANLG
SCALE	[10] :	80 dB
BANDWIDTH	[16] :	1.74 kHz
AVRG	[11] :	ON
f_{START}	[7] :	9.000 000 MHz
f_{STOP}	[7] :	9.000 002 MHz
SWEEP TIME	[17] :	0.1 s
SWEEP∿∿	[13] :	ON
RANGE	[8], [9] :	0 dB/dBm

8600 A:

FUNCTION	:	DCV
RANGE	:	20 V

Vary the send level at the PS-19 so that the level line on the SG-4 coincides precisely with the 0 dB/dBm graticule line. Read off the corrresponding Y-voltage on the DVM.

Check the following points specified in the table:

SPM-19 SCALE [10]	SG-4 Graticule line to be checked (dB/dBm)	PS-19 Send level [2], [3], [4] (dB/dBm)	DVM (Y-voltage) Setpoint value	DVM (Y-voltage) Error limits (e)	Error of measuring setup (m)
80 dB	0	approx.0	5.000 V (≅ 0 dB)	±50 mV (≅ ±0.8 dB)	±5 mV
	-30	approx.-30	3.125 V (≅ -30 dB)		
	-60	approx.-60	1.250 V (≅ -60 dB)		
20 dB	0	approx.0	3.972 V (≅ 0 dB)	+93 -90 mV (≅ ±0,2 dB)	±5 mV
	-5	approx.-5	2.234 V (≅ -5 dB)	+52 -51 mV	
	-10	approx.-10	1.256 V (≅ -10 dB)	+74 -70 mV (≅ ±0,5 dB)	
	-15	approx.-15	0.706 V (≅ -20 dB)	+42 -39 mV	
1 dB	0.5	approx.0.5	5.458 V (≅ 0.5 dB)	+92 -92 mV (≅ ±0.03 dB)	±5 mV
	0	approx.0	3.972 V (≅ 0 dB)	+86 -87mV	
	-0.5	approx.0.5	2.570 V (≅ -0.5 dB)	+82 -82 mV	
	-1.0	approx.-1.0	1.247 V (≅ -1.0 dB)	+78 -77 mV	

Figure 8-2 Table to demonstrate the error characteristics of the SG-4

In the 1 dB scale range, the 0.1 dB divisions of the PS19 are not sufficient to position the level line on the SG-4 precisely over a particular graticule line.

The following procedure should therefore be followed:

- Vary the output level at the PS-19 so that the level line is just above the corresponding graticule line.
- Reduce the frequency of the PS-19 with MAN FINE [17]. As a result of the 1.74 kHz bandwidth filter, the level line drops.
- Adjust the frequency of the PS-19 so that the level line coincides precisely with the desired graticule line.

Note:
By means of the cursor line on the SG-4, other arbitrary points can be inspected. Formulae for calculating the setpoint value of the Y-voltage:

80-dB scale range: $5{,}000\ V \cdot \left(1 + \frac{L}{80\ dB}\right)$

20-dB scale range: $3{,}972\ V \cdot 10^{\frac{L}{20\ dB}}$

1-dB scale rangech: $24{,}7737\ V \cdot \left(10^{\frac{L}{19{,}7653\ dB}} - 20{,}802\ V\right)$

L: level value of the cursor/graticule line

9 DESCRIPTION OF FUNCTIONS AND CIRCUITRY

9.1 FUNCTIONAL DESCRIPTION OF THE ENTIRE UNIT

The SG-4 Display Unit can be used to extend Level Meters SPM-16 and SPM-19, which are capable of sweep operation, to panoramic receivers or, in conjunction with a level generator, to sweep measuring systems. The Display Unit displays the sweep curve as a stationary trace, even at low frequencies. The SG-4 is therefore particularly suitable for taking measurements on specimens with slow rise times and for displaying the spectral lines or system occupancy of carrier-frequency (FDM) systems. Its characteristics also allow comparative measurements, normalizer mode, the measuring of signal drift or end-to-end sweep measurements with unsynchronized senders. The standard IEC (IEEE) interface enables operation in computer-controlled measuring systems.

9.1.1 FUNCTIONAL SEQUENCE

With a parameter entry the Selective Level Meter, the program in the Selective Level Meter runs through the interpretation and then issues an interrupt request to the Display Unit.

The SG-4 fetches the "image data" (via the IEC bus), processes these into an inscribed graticule and displays them on the 7" monitor. The X- and Y-output voltages are continuously digitized in the SG-4 and stored in a memory. After processing of these signals by the CPU, the digitized values are displayed on the computed graticule. The result is a stationary image.

9.1.2 LIST OF MODULES

No.	BN	Letter	Abbreviated designation	Designation
(1)	844		NNT-3	Power supply
(2)	957	C	SG-4	Entry circuit
(3)	957	B	SG-4	Convertor card
(4)	957	A	SG-4	Buffer memory
(5)	957	D	SG-4	Wiring card
(90)	965	A	CPU-2	Processor card
(91)	958	A	IEC 625	IEC bus card
(92)	962	A	BSK-1	CRT control card
(93)	980/01	A		7" monitor

9.1.3 ENTRY CIRCUIT

The keyboard is connected in matrix fashion. A key stroke triggers an interrupt (RST 5,5). The program detects the key number and changes the display accordingly.

9.1.4 CONVERTOR CARD

The X-voltage from the Level Meter is digitized with 1/512 resolution and presented to the buffer memory in the form of addresses.

Depending on the level range in the Selective Level Meter, the Y-voltage is fed to the Y-convertor (1/256 resolution) either directly or via the 2 dB or 20 dB logarithmizer. The digital values thus obtained are stored as data in the buffer memory.

For the X-voltage conversion, automatic gain and offset alignment is additionally provided in order to compensate for tolerances of the Level Meter. This is dispensed with for Y, because the Selective Level Meter is calibrated at the output.

9.1.5 BUFFER MEMORY

The minimum and maximum values are formed within an X-value from the data supplied by the convertor card, and stored in the RAM before the address change. Furthermore, other values such as sweep out/return, new value, pen up/down are stored in a check byte. The storage area required in the buffer memory is 3 x 512 x 8 bits. During reading out of the buffer memory, the check byte is deleted to detect whether the storage location has been reloaded since the last read operation. The read operation itself increments the address counter so that only one response address is required.

9.1.6 SUBSEQUENT PROCESSING OF THE DATA

The pairs of values now stored in the processor are subjected to further processing there and displayed on the monitor, depending on the mode.

The numerous remaining functions are exclusively implemented by software.

9.2 CIRCUITRY DESCRIPTION OF THE MODULES

9.2.1 POWER SUPPLY NNT-3 BN 844 circuit diagram (1)

The main sections of the power supply are the a.c. power input with connector, fuse with fuse holder, voltage selector and a.c. line filter, transformer, rectifier circuit, smoothing and regulation circuitry.

The individual secondary voltages transformed in the power transformer are rectified, smoothed and applied to the regulators.

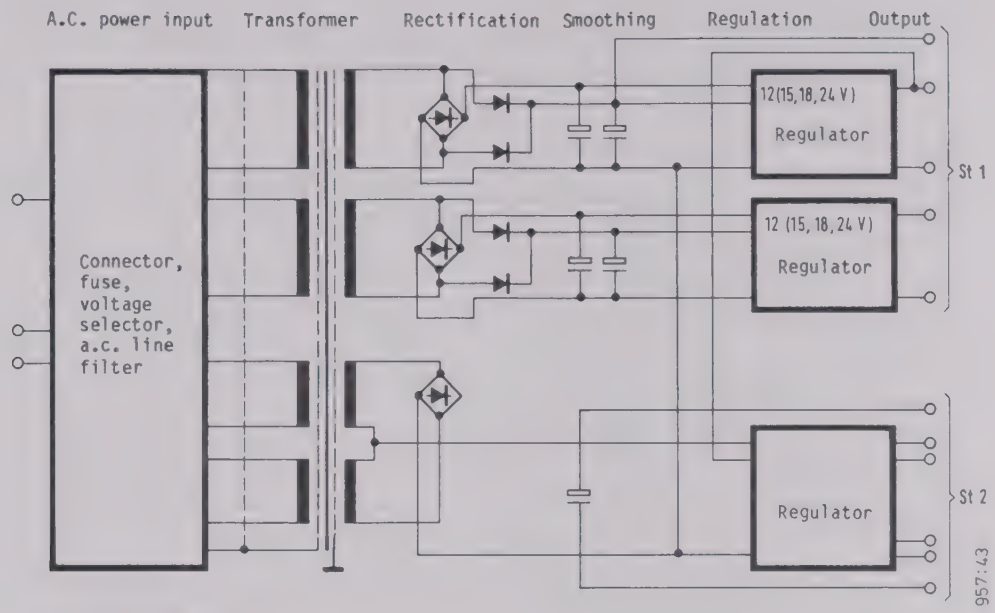
For the $\pm$ 12 V (15 V/18 V/24 V) regulators, the auxiliary voltage is obtained on the a.c. side from the supply voltage for the regulators via their own rectification and smoothing circuits.

The auxiliary voltage for the 5 V regulator of the NNT-3 is obtained from the regulated +12 V (+15 V, +18 V, +24 V) output voltage.

With the standard power supply, there is a facility for obtaining the rectified and smoothed voltage (upper voltage) from the smoothing capacitor at the output for the +5 V, +12 V (+15V/ +18 V/+24 V) voltage.

The sensor lines for the 5 V voltage are wired to output St 2 separately from the main conductors. The individual output voltages can only be subjected to their maximum currents when the remaining voltages are unloaded or only partially loaded.

Block diagram:



Standard regulator IC

Types:

The following types are possible:

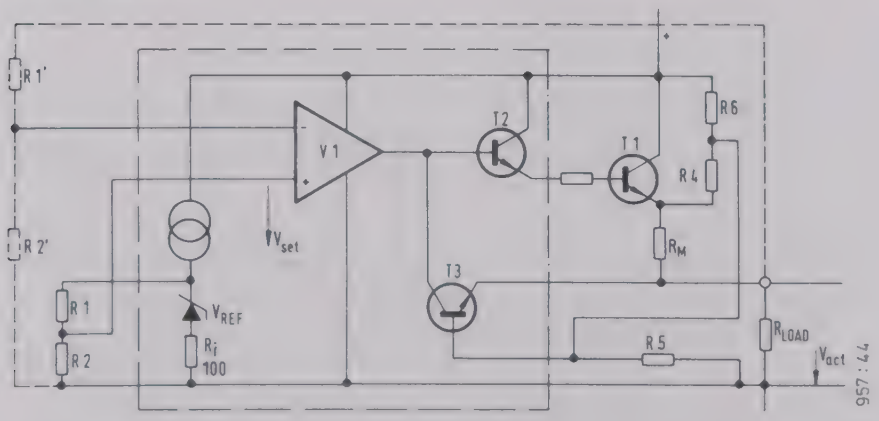
5 V, 12 V, 15 V, 18 V, 24 V

$I_L \leq 1.30$ A regulator L 123 + transistor stage MJE 3055

$I_L \leq 4.00$ A regulator L 123 + transistor stage BSX 45-16 + 2 MJE 3055 in parallel.

Regulator L 123 is an integrated circuit chip in a TO 100 case.

Mode of operation:



The circuit of the standard regulator consists of the following stages:

a) Differential amplifier V_1 in the L 123-T1 IC chip compares the actual value of the output voltage with the setpoint voltage present at voltage divider R1/R2. The voltage divider is supplied with the integral reference voltage V_{REF} in the IC.

b) The control element (T2 in the IC and T1 externally) in cascade configuration is driven by differential amplifier V_1.

c) The current limiting circuit (R4, R5, R6, R_M and T3) protects the control element from thermal overload in the event of a short circuit at the output.

After the regulator has been switched on, the positive voltage V_{set} builts up at the + input of differential amplifier V_1. At this time, the control element is still turned off and the output voltage is equal to 0. Since the "-" input of the differential amplifier receives no voltage from the output, and the "+" input is positive as a result of "V_{set}", the output of the differential amplifier is driven in the positive direction and the control element therefore conducts. It continues to conduct until the output voltage at the load resistance V_{ACT} is the same as voltage V_{set}. On account of the high gain, the voltage required to drive the amplifier is negligible. Resistors R4, R5, R6 and R_M are chosen so that at rated current I_R transistor T3 is off and has no effect on the regulating characteristics of the circuit. If the load current rises, the base-emitter voltage of transistor T3 rises also. This transistor starts conducting at $2...3 \cdot I_R$ and draws the control current of the control element, so that the current in the control element decreases and the output voltage collapses. This collapse is assisted by the rise in current in R6, which additionally increases the base current of T3. This achieves an output current foldback in the event of overload. The regulator is short circuit-proof for 1 minute; operation at 2..3 times the rated current (just before the knee of the characteristic curve) is not permissible. After removal of the short circuit or overload, the output voltage is automatically restored.

The output voltage level is governed by voltage divider R1/R2 via the reference voltage. This is only possible as long as the output voltage is equal to or less than the reference voltage. For the 12 V, 15 V, 18 V, 24 V series, the reference voltage V_{ref} is applied to the "+" input of the differential amplifier without division, whilst the voltage fed back from the output of the control element is applied via a divider to the "-" input of the amplifier. The output voltage is then greater than V_{ref} by the factor $(1+\frac{R1'}{R2'})$.

9.2.2 ENTRY CIRCUIT circuit diagram (2)

9.2.2.1 Keyboard and key debounce circuit

In the quiescent state, all outputs of IC 7 are at logic LOW, whilst the inputs of IC 6 or IC 8 are at +5 V via R6 (10 kΩ). If a particular key is pressed, an input of IC 8 is connected to an output of IC 7 via the key and thus placed at logic LOW. Thus IC 8.13 = H and activates the key debounce circuit.

The key debounce circuit nullifies the effect of the bounce caused by pressing and releasing a key. If IC 8.13 = H, counter IC 10.1 ... 7 starts counting (input frequency≈350 Hz). It is reset each time that IC 8.13 briefly goes to logic LOW on account of a bouncing key. Once the bounce is over, the counter finally reaches count status "8"; Q 3 = IC 10.6 = H. The positive transition at IC 10.6 triggers IC 9 and the key interrupt line goes to logic HIGH. If the key is released, counter IC 10.9 ... 15 starts counting. When it reaches count status "8" (Q 3 = H), it sets counter IC 10.1 ... 7 to zero and the next pressed key can be registered.

The key interrupt line (logic H) prompts (on the convertor card) the processor via line RST 5.5 to scan the keyboard. In order to detect which key is currently pressed, the processor sets one output of IC 7 after the others at logic LOW, whilst the remaining are at HIGH (address 39H), and scans the input states of IC 6 (address 3 A). IC 9 is then reset (address 3BH).

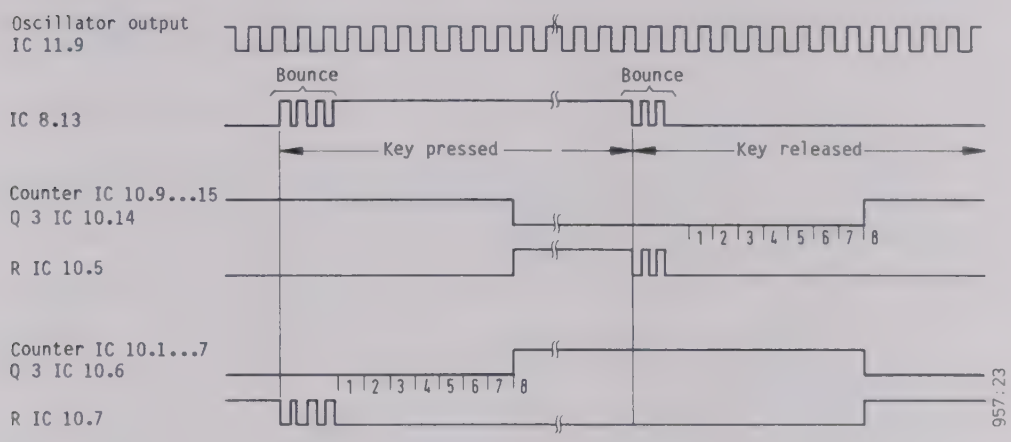


Figure 9-1 Pulse diagram of the key debounce circuit

9.2.2.2 Port assignments of the input circuit

The following table shows the port assignments of the input circuit.

Designation	Label/ address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LEDs/3	30 ... 33	-	Gl 30	Gl 22	Gl 21	-	Gl 19	Gl 18	-
LEDs/2	34 ... 37	Gl 16	Gl 15	-	Gl 13	-	Gl 11	Gl 10	-
LEDs/1	38	Gl 1							
Keyboard column	39	scan corresponding column							
Keyboard rows	3A	L	L	Key pressed					
Key interrupt reset	3B								

Figure 9-2 Port assignments of the input circuit

9.2.3 CONVERTOR CARD circuit diagram (3)

For the measured signals, the convertor card is the interface with the Selective Level Meter. It receives the analog Y-signal (= level) and the analog X-signal (= frequency) from the Level Meter and prepares both signals for digital processing. The tasks of the convertor card are as follows:

1) The analog Y-signal is logarithmized on the convertor card (1 dB and 20 dB range) in accordance with the selected measuring range of the Level Meter, or directly routed (80 dB range).
2) The Y-signal is converted from analog to digital and presented to the buffer memory card as an 8-bit wide data word (Y0 ... Y7).
3) The analog X-signal is fed to an A/D convertor, via a lowpass filter for interference suppression, and is presented to the buffer memory card as a 9-bit wide data word (XA 3 ... XA 11).
4) A self-test is implemented in order to check the A/D convertor and the buffer memory card which follows.
5) The signals "address change", "BA" and "erase check byte" are generated for control of the buffer memory card.
6) The interrupt requests from the input circuit, CRT control card, and Selective Level Meter are routed to the processor card via the convertor card.

9.2.3.1 Y-channel

The Y-voltage from the Level Meter is logarithmized in the Y-channel as required and then subjected to A/D conversion. The extent of the display on the screen of the SG-4 should be approximately the same as on the analog meter of the SPM-19 Level Meter.

20 dB logarithmizer

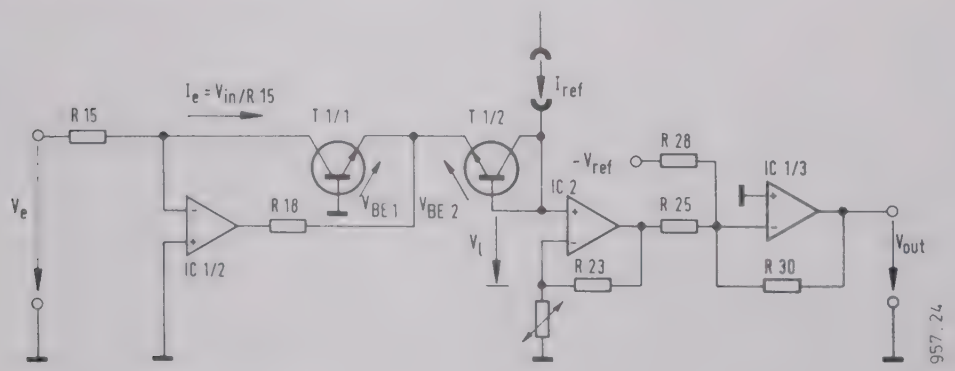


Figure 9-3 20 dB logarithmizer

This is a characteristic curve logarithmizer. The equation for a diode characteristic $I_0 = f(V_D)$ is

$$I_D = I_{SO} \exp\left(\frac{V_D}{V_T}\right) \text{for } V_D \gg V_T.$$

This relationship is utilized. After passing through buffer stage IC 1/1, the Y-signal reaches the actual logarithmizer IC 1/2, T 1/1. A proportional current I_E is obtained from the input voltage V_{in}; this current flows through the collector-emitter junction of T 1/1. The base-emitter voltage of T 1/1 is given by: $V_{BE1} \sim \log I_e/B \cdot I_{so}$. Logarithmizing takes place at the base-emitter diode of T 1/1. A dual transistor is used for T 1. The constant reference current I_{ref}, which is produced by means of IC 3/4 and T 2, flows through the second transistor T 1/2. The voltage at the non-inverting input of IC 2 is

$$V_L = V_{BE2} - V_{BE1} = -v_T \log \frac{I_E}{I_{ref}}.$$

As a result of the circuit chosen, which makes use of a dual transistor, the influence of I_{so} on the output voltage V_1 is removed; thus the temperature-dependence of I_{so} is no longer an interfering factor. Amplifier IC 2 follows. The temperature-dependence of v_T is compensated for by the temperature-dependent resistance R_r which is created by R 19, R 20 and R 24. Inverter IC 1/3 produces the correct polarity of the output voltage V_{out}.

The Display Unit should exhibit greatest accuracy at the display range around 0 dB $\cong V_{in}$ = 3.972 V. The reference current I_{ref} has been chosen (80 µA) so that the input voltage of IC 2 is V_1 = 0 V at V_{in} = 3.972 V; thus the amplification errors of IC 2 in this range have no effect. By means of R 28 and IC 1/3, a particular amount is added to the output voltage of IC 2 so that the relationship between input voltage V_{in} and output voltage V_{out} is correct.

2 dB logarithmizer

A diode function network is used which approximates the logarithmic characteristic curve by a knee characteristic curve. In principle it is a voltage divider with which resistors are switched in parallel with resistor R 6 as the output voltage V_{out} rises, so that the divider ratio is reduced. The resistors are connected to the output voltage V_{out} via diodes, and the cathodes of the diodes have different positive bias. If the output voltage V_{out} is greater than the bias voltage plus the threshold voltage of a diode, the latter conducts; the corresponding resistor is in parallel with R 6.

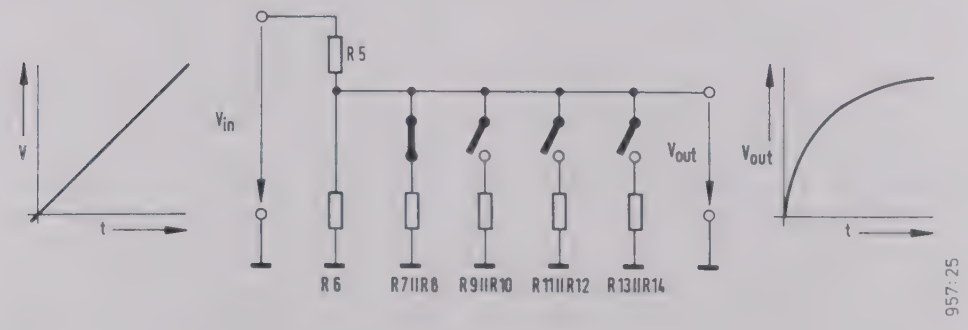


Figure 9-4 2 dB logarithmizer

Range switching and test functions

Three ranges of readings can be selected on the SPM-19 Level Meter: 1 dB, 20 dB and 80 dB ranges. In the SG-4, brancher IC 4 switches the corresponding signal path for the Y-signal to the A/D convertor. The following table shows the relationships:

Range of readings Level meter	Y-signal path SG-4	A/D convertor output 1 LSB ≡	Control inputs Brancher IC 4 C B A	Port 14H Bits 3 ... 0
1 dB	2 dB log.	0.01 dB	L H L	E H
20 dB	20 dB log.	0.1 dB	L L H	D H
80 dB	80 dB path (direct connection)	1/3 dB	L L L	C H
Test SG-4	+5.5 V/-0.5 V		H/L H H	3 H

Figure 9-5 Display ranges of the SG-4 and test function

In the 80 dB range, the Level Meter delivers a logarithmic Y-signal which is directly applied to the A/D convertor in the Display Unit via brancher IC 4. The latter is controlled by the processor by way of port IC 32 (address 14H).

A self-test facility is implemented in the SG-4. The two voltages +5.5 V and -0.5 V are alternately switched via IC 4 to the A/D convertor of the Y-channel. Since both voltages are beyond the normal voltage range of the A/D convertor (0 ... 5 V) and are switched over periodically (at 656 Hz), the A/D convertor alternately travels to the upper and lower ends of the range at maximum speed. A periodically repeating bit pattern is obtained at the digital outputs, which can be checked by means of signature analysis. The self-test is switched on by the processor via port IC 32; counter IC 34 is also enabled (IC 34.11), which periodically switches over the two test voltages (IC 34.4 - IC 33.9 - IC 4.9) by way of IC 34.3 and IC 33.5. Counter IC 34 causes the X-convertor to count up and down periodically.

Y-convertor

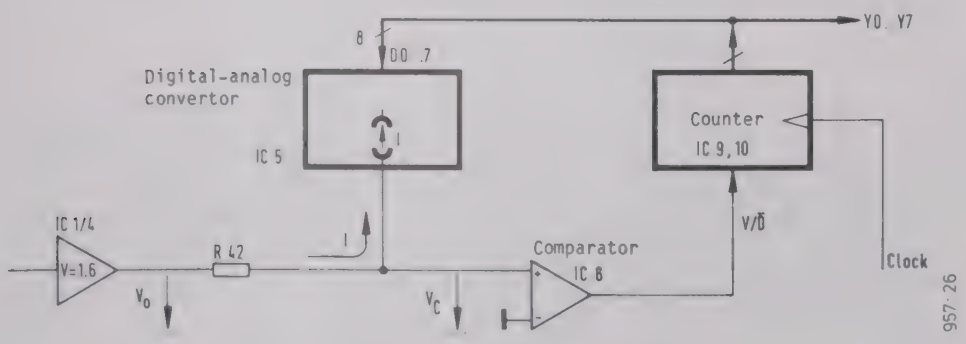


Figure 9-6 Tracking convertor of the Y-channel

The Y-signal voltage from brancher IC 4 is 0 ... 5 V. It is amplified to 0 ... 8 V by amplifier IC 1/4 (V = 1.6).

An 8-bit follow-up convertor is used as A/D convertor for the Y-signal. In order to explain its function, it is assumed that the input voltage V_o of the A/D convertor increases suddenly. Thus $V_C > 0$ V and the comparator uses signal V/$\overline{D}$ to prompt the counter to count up. The current source of the digital-analog convertor allows a current I to flow which is proportional to

the digital value presented. As the counter status increases, current I also increases and voltage $V_C = V_o - R_{42} \cdot I$ decreases. When $V_C = 0$ the comparator terminates the up-counting of the counter. The counter status is the digital value of the Y-signal V_o; it is rerouted to the buffer memory card.

The tracking convertor exhibits no hysteresis; the output signal $V/\overline{D}$ of the comparator can only assume the two states "count up" or "count down". If the tracking convertor is in the stationary state, the counter continuously counts one step up and down. The digitized Y-signal continuously toggles back and forth between two adjacent digital values.

The time required for a complete cycle of the convertor (0 ... 255) is approximately 0.61 ms. The output signal of the comparator is synchronized by means of flipflop IC 7. By way of gate IC 8.11 ... 13, the carry-output IC 10.15 causes the counter IC 9, 10 to stop at the upper and lower ends of the range.

9.2.3.2 X-channel

Lowpass filter and changeover switch with test function

The X-signal from the Level Meter (-2.5 V ... +2.5 V) is fed to an active second-order lowpass filter IC 3/1 which rejects interference. The signal is then fed via brancher IC 13/1, with which the test function can be switched on, to the analog-digital convertor of the X-channel.

The self-test in the X-channel is switched on together with the test in the Y-channel by the processor via port IC 32 (address 14H); in normal mode IC 13.10 = H, and in test mode IC 13.10 = L. Counter IC 34 periodically switches (2.5 Hz) the two voltages ± 3.1 V through to the A/D convertor (IC 34.3 - IC 33.5 - IC 13.9).

The A/D convertor of the X-channel alternately runs to the upper and lower ends of the range at maximum speed. Counters IC 19, 21, 23 count up in BCD code and count down in binary code. The changeover is performed by counter IC 34 via IC 35/1 ... 3 (up-counting: IC 34.3 = IC 33.5 = IC 35.13 = L; down-counting: IC 34.3 = IC 33.5 = IC 35.13 = H). In test mode, the "pen down" signal from the Level Meter is replaced by the signal at IC 13.1.2.9; switching is performed by brancher IC 13/2. When test mode has ended, the signal IC 32.10 = H sets counter IC 34 to zero and ensures via IC 35.11 = L, IC 35.13 = H that the X-A/D convertor can only count in binary code.

X-convertor

From the changeover switch the X-signal is fed to amplifier IC 3/3 which converts the voltage range ± 5 V to 0 ... 8 V. The X-A/D convertor which follows operates as a tracking convertor with a resolution of 9 bits. The main elements are a 12-bit up/down counter, a 10-bit D/A convertor, a comparator to detect the direction and a circuit to detect an impending change of outputs XA3 ... 11 (address change detection).

For the sake of simplicity it is first assumed that the inverting input of the comparator IC 14 is at ground potential. The tracking convertor then operates similarly to the Y-convertor; see description of the latter. It differs from the Y-convertor as follows:

- The three lowest-order counter outputs (XA 0 ... 2) are not rerouted to the buffer memory card.
- Counter outputs XA 0, 1 are not rerouted to the D/A convertor. The counter must count another 4 steps until the LSB (XA 2) changes at the inputs of the D/A convertor and, as a result of current I and voltage V_{C+}, at the comparator.

- The output signal "V/$\overline{D}$" of the comparator which establishes the counting direction of the counter is delayed by one clock period by flipflop IC 17/1. If the digital input value of the D/A convertor changes (XA 2 ... 11), and if the comparator consequently switches over the counting direction, the counter counts one more step in the original direction as a result of the delay of signal "V/$\overline{D}$".

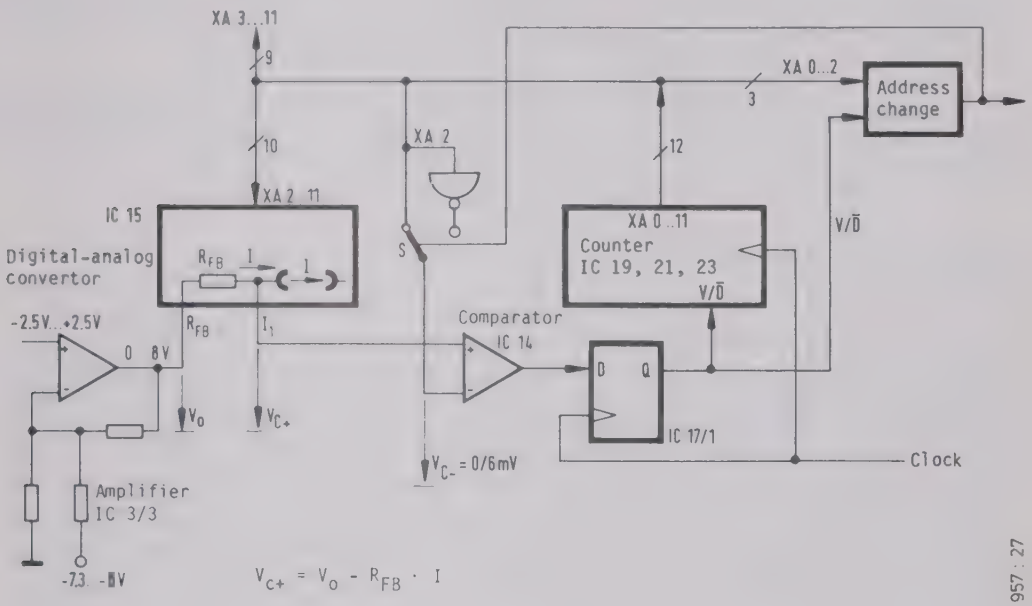


Figure 9-7 Tracking convertor of the X-channel

The implemented X-convertor exhibits hysteresis, caused by switching of the voltage at the inverting input of the comparator between 0 and 6 mV by signal XA 2. Figure 9-9 shows the basic operation of the hysteresis. With XA 2 = L, V_{C-} = 0 mV; the comparator is prompted to let the counter count up. With XA 2 = H, V_{C-} = 6 mV; the counter is prompted to count down. As shown in Figure 9-9 (arrows) the counter is influenced by V_{C-} in such a way that the counter status must remain at the midpoint between two address changes. If an address change takes place, V_{C-} already changes its state with the address change signal at IC 29.4 via IC 29/1. This improves the signal-to-noise ratio. Referred to X-signal $\pm$ 2.5 V from the Level Meter, the hysteresis is approximately 2 mV at an input voltage of -2.5 V, and up to approximately 6 mV at an input voltage of +2.5 V. Figure 9-8 shows the pulse diagram of the X-convertor for the stationary state. During the transition from XA 3 ... 0 = 7 to XA 3 ... 0 = 8 an address change takes place. The next address change would be between XA 3 ... 0 = F and XA 3 ... 0 = 0. Since, however, V_{C+} < 6 mV, the counter swings between XA 3 ... 0 = A and XA 3 ... 0 = D. With XA 3 ... 11, which are rerouted to the buffer memory card, no change takes place.

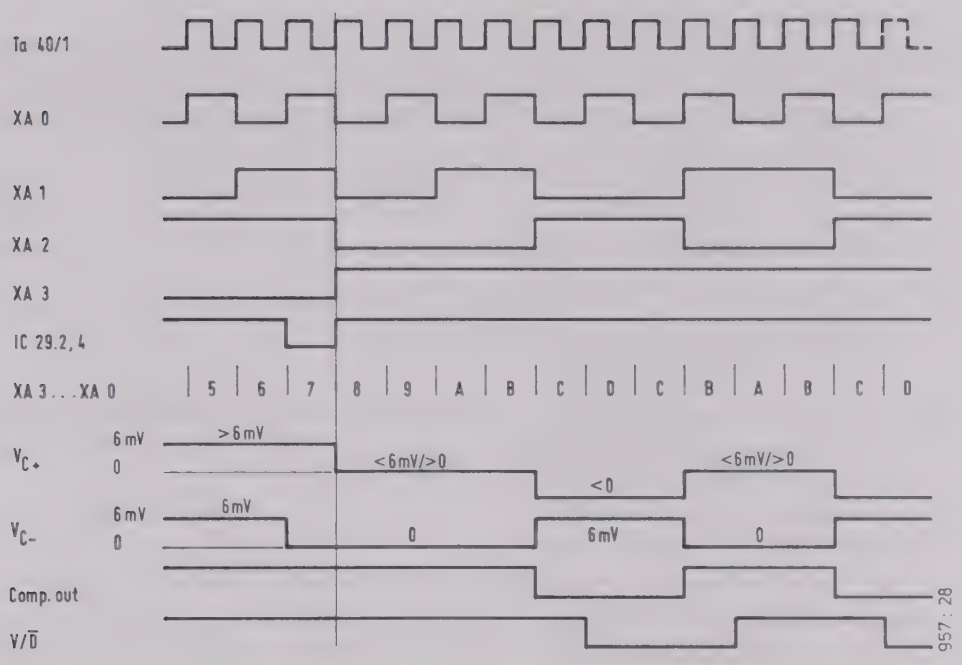


Figure 9-8 Pulse diagram of the X-tracking convertor

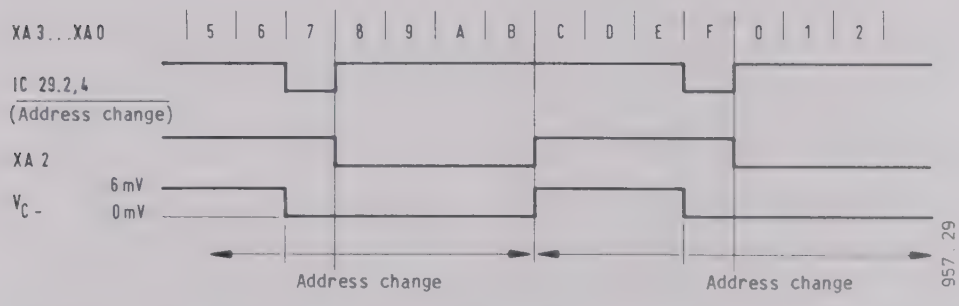


Figure 9-9 Basic operation of the hysteresis (signals IC 29.2.4 and V_{C-} during up-counting)

With the mode described above, the X-convertor follows an X-signal with random fluctuation as is required during manual frequency adjustment on the Level Meter (port address 1A H, bit 4 = H; IC 26.6 = IC 25.4 = H). During sweep mode, the counter of the X-convertor may only count up with the sweep out direction ("Pen down" signal from the Level Meter = H) and may only count down with the return direction ("Pen down" = L) (IC 26.6 = L). EX-NOR gate IC 29/3 compares the "Pen down" signal from the Selective Level Meter with the "V/$\overline{D}$" signal which indicates the present counting direction of the counter. If these agree, the clock signal is enabled via IC 26.5 = IC 25.4 = H. In test mode, the "Pen down" signal is simulated by way of brancher IC 13/2 (address 14 H, bit 4). When the counter reaches its final value, it is inhibited by IC 25.3 = L. The period for a complete cycle of the X-convertor is 98 ms.

Calibrating the X-channel

The Level Meter delivers the voltages -2.5 V and +2.5 V for calibration of the X-channel. The processor scans the digital X-values via the buffer memory card. If these differ from the set-point values, it uses D/A convertors IC 12 and IC 16 to correct the offset (address 10 H) and the gain (address 11 H) of the X-channel. The offset adjustment is made via amplifier IC 3/3. The reference voltage of the D/A convertor IC 15 can be varied over the range -7.3 V ... +8.7 V to adjust the amplifier.

9.2.3.3 "Address change" and "BA" signals with various modes

The "address change" signal causes the digital Y-value to be stored. The counter of the X-convertor supplies an address change pulse in the event of an impending change of the X-value. The logical condition is:

(XA 0 = XA 1 = XA 2 = H and V/$\overline{D}$ = H) or
(XA 0 = XA 1 = XA 2 = L and V/$\overline{D}$ = L) and
counter not at initial status.

This condition is implemented by IC 27/1, IC 28/1 and IC 29/2. IC 30 combines the address change pulse with the clock signal and also affects it as required.

Signal "BA" = H enables the buffer memory for storage of the Y-values, and "BA" = L inhibits it. Thus, during sweep out only or during sweep return only, it is possible to control the moment when Y-values are to be stored and displayed on the screen. It is also possible, alternately with a certain number of sweep cycles (1, 2, 4 or 8) to store and display the Y-values only during the sweep out and then, with the same number of cycles, only during the sweep return. Counter IC 24 counts the sweep cycles. If, for example, alternating is always to take place between the displaying of sweep out and sweep return after 4 sweep cycles, brancher IC 22 switches output Q_2 of IC 24 to the EX-NOR gate IC 29/4. The comparison with the "Pen down" signal (H for sweep out, L for sweep return) produces the "BA" signal.

"Manual frequency adjustment" mode

The processor selects the value 48 H at port IC 18 (address 1A H). By means of bits 2 ... 0 = L, brancher IC 22 is switched so that the same "Pen down" signal is present at both inputs of the EX-NOR gate IC 29/4. "BA" is constantly at logic HIGH so that storage can take place with each address change pulse. Bit 3 = H from port IC 18 enables the counter of the X-convertor to count up and down as required by the X-signal. As a result of bit 4 = L and bit 5 = L, IC 30.2 = IC 30.13 = IC 30.11 = L, so that the address change pulses from the counter of the X-convertor can pass and be fed to the buffer memory card. Since bit 6 = H, the check byte is set to zero when the buffer memory is scanned (see Section 9.2.4.4).

"Sweep" mode

At slow sweeps of the level meter ($\geq$ 3 s) the value 40 H is present at port IC 18. The Y-values are stored with each address change pulse. Since bit 3 = L, the counter of the X-convertor only counts in the sweep direction; its address change pulses are fed to the buffer memory card (bit 4 = bit 5 = L). The check byte is set to zero.

If the Level Meter sweeps faster, 67 H is present at port IC 18. Bit 0 = bit 1 = bit 2 = H causes output XA 3 of the X-convertor to be applied via IC 22 to the EX-NOR gate and compared with the "Pen down" signal. In the sweep out, the Y-values are only represented at odd X-addresses,

and in the sweep return only at even X-addresses. Thus both measuring curves are displayed simultaneously, though with half the X-resolution. The result of bit 5 = H is that address change pulses only reach the buffer memory card when "BA" = H (IC 35.3 = L; IC 35.5 = L with "BA" = H).

"Step" mode

18 H is present at port IC 18. The Y-values are stored with each address change pulse. Via IC 27.5 = IC 30.2 = H, bit 4 = H causes the address change pulses from the X-convertor to be inhibited and the "Pen down" signal to be used instead. The check byte is not set to zero.

9.2.3.4 Interrupts

The interrupt requests "Int 1" from the CRT control card and "Int. SG-4" from the Level Meter are stored in the flipflops of IC 37. "Int. SG-4" affects the processor via line "RST 6,5"; "Int 1" and the key interrupt via line "RST 5,5". By way of port IC 20/2 (address 16 H), the processor queries which interrupt has been activated. The flipflops are reset by addresses 17 H and 18 H.

Designation	Label Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X-offset	10	← binary coded (correction value) →							
X-gain	11	← binary coded (correction value) →							
	12								
	13								
Input change-over	14	← free →				coded (see supplementary sheet)			
Pen down/up (out/return)	15	← free →						Pen down	Pen up
INT	16	INT SG-4	INT 1 ← free →						
Reset INT 1	17								
Reset INT SG-4	18								
	19								
Mode	1 A	free	delete kbyte	address change	address change with step mode	X-conv mode	sweep out/return	display	
Sweeps	1 B	← free →				2^3 ← sweeps →			2^0

Figure 9-10 Port assignments of the convertor card

9.2.3.5 Port assignments of the convertor card

Figure 9-10 shows the port assignments of the convertor card. The following is additional information:

X-offset: } correction values for the X-calibration
Y-gain: } are entered via the addresses.

Input changeover:

Bit 7	6	5	4	3	2	1	0	Hex.	Function
				H	H	L	L	Ø C	80 dB path
				H	H	L	H	Ø D	20 dB log.
				H	H	H	L	Ø E	2 dB log.
				L	L	H	H	Ø 3	test
				H	L	H	H	Ø B	test off

Figure 9-11 Input changeover

Pen down/up: The processor scans the "Pen down" and "Pen up" signals from the Level Meter. The signals are normally inverted with respect to each other. If both signals = LOW, the processor is aware that the Level Meter is switched off.

INT: The flipflops of Interrupt 1 and Interrupt SG-4 are scanned.

Reset INT 1: } The corresponding flipflops are
Reset INT SG-4: } reset.

Mode: see Figure 9-12 and the description in Section 9.2.3.3

Bit 7	6	5	4	3	2	1	0	
								storage of the curves for the sweep out and return directions (via signal "BA")
					L	L	L	always
					L	L	H	alternating after 1 cycle
					L	H	L	alternating after 2 cycles
					L	H	H	alternating after 4 cycles
					H	L	L	alternating after 8 cycles
					H	L	H	sweep out only
					H	H	L	return sweep only
					H	H	H	sweep out with odd X-values, return sweep with even X-values
				L				X-counter counts in sweep direction only
				H				any
			L					address change from X-convertor
			H					address change with step mode
		L						address change from X-convertor with each X-address
		H						only with "BA" = H
	L							check byte is not set to zero during scan
	H							set to zero

Figure 9-12 Selecting various modes

Sweeps: Counter IC 24 counts the sweep cycles. The counter status can be scanned via this address.

9.2.4 BUFFER MEMORY CARD circuit diagram (4)

From the convertor card, the buffer memory card receives the digitized Y-signal YO ... 7 and the digitized X-signal XA 3 ... 11, the information on the counting direction of counters V/$\overline{D}$(X) and V/$\overline{D}$(Y) and some control signals. The following processes take place:

1) The processor scans the current values of YO ... 7 and XA 3 ... 11, in order to display the instantaneous values of level and frequency on the screen as a marker.
2) Several Y-values YO ... 7 usually appear within one X-value XA 3 ... 11. Of the Y-values appearing within one X-value, the maximum and minimum are therefore formed and subsequently written into the buffer memory. The X-value serves as storage address. Thus the entire measuring curve is stored in the buffer memory.
3) The processor periodically reads out the measuring curve located in the buffer memory. The buffer memory is addressed by the address counter.
4) When settings of the Level Meter or of the SG-4 are varied, the buffer memory is cleared.
5) The clock generator for the convertor and buffer memory cards is located on the buffer memory card.

9.2.4.1 Present values

The instantaneous values of frequency and level are displayed on the screen by means of a marker. For this purpose, the processor requires the current X and Y-values arriving from the convertor card. By means of the IO address "Current value/1" (address 28 H), the instantaneous values of XA 3 ... 11, YO ... 7, V/$\overline{D}$(X), V/$\overline{D}$(Y) and "Sweep out/$\overline{return}$" are loaded into registers IC 5, 39, 45 and the values XA 3 ... 10 (IC 45) are applied to the data bus. IC 46 synchronizes the "Current value/1" signal. The processor is stopped during this time by the signal "Ready" = L. Using the addresses "Current value/2" and "Current value/3", the processor subsequently scans the remaining present values (IC 39, 5).

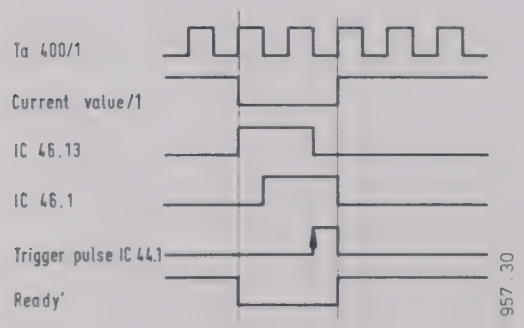


Figure 9-13 Sequence for "Current value/1"

9.2.4.2 Maximum value formation and minimum value formation with writing-in

The Y-data Y0 ... 7 are used for maximum value and minimum value formation. The maximum and minimum of the Y-data appearing during one X-value are established here. If a change in X-value is announced by the "Address change" signal, the instantaneous Y-value is transferred to the memory for maximum value formation IC 10 and to the memory for minimum value formation IC 7. Until the next address change, the Y-data are continuously compared with the contents of these two memories (comparators for maximum value formation IC 11, 12, minimum value formation IC 8, 9). If the instantaneous Y-value is greater than the value stored in the maximum value memory (IC 10) (IC 16.9 = L), it is stored in the maximum value memory as a new maximum value. The process for minimum value formation is analogous. Thus the maximum or minimum of all Y-values since the last address change are always in the two memories IC 10 and IC 7 respectively. The new address change pulse toggles three tri-state flipflops so that the maximum is stored in IC 21, the minimum in IC 22 and the check byte in IC 23. The address change pulse again causes the instantaneous Y-value to be transferred to the maximum value memory IC 10 and the minimum value memory IC 7 (signal path:
"Address change" = H - IC 31.11 = L - IC 16.6 = H - IC 6.1.6 = L, Ta 400/2 at IC 7.11 and IC 10.11.)

Furthermore, the address change pulse causes the maximum, minimum and check byte - located in IC 21, IC 22 and IC 23 - to be written into the buffer memory (RAM IC 38). During the address change pulse, IC 18.1 = H, so that the clock signal Ta 400/1 enables decoder IC 3/2, and IC 19.1 = L, so that counter IC 19 is enabled. IC 19 counts the clock pulses of Ta 400/2; its counter status is decoded (IC 3/2). Thus the outputs of IC 21, IC 22 and IC 23 are activated successively and the maximum, minimum and check byte are applied to the data pins of the RAM.

The address change pulse takes place during $\overline{\text{Ta 40/1}}$ = H. Via IC 31.4 ... 10, $\overline{\text{Ta 40/1}}$ = H switches over the changeover switch IC 35 ... 37, so that the RAM address bits 0 and 1 are determined by counter IC 19, and the RAM address bits 2 ... 10 are determined by the X-value XA 3 ... 11. Via IC 30.5 = L, IC 30.9 = H, IC 30.12 = L and IC 42.2 = H, the address change pulse enables the write pulses for storage of maximum, minimum and check byte at the RAM input $\overline{\text{WE}}$. A precondition is that the write pulse is enabled (IC 30.10 = H) by means of the IO address "Inhibit memory" in conjunction with DO = H (IC 43.1 = H), and by the signal BA = H from the convertor card. If one of the preconditions is not met, IC 30.10 = L and the RAM reads out. Then IC 18.5 = L, decoder IC 3 is inhibited and the outputs of flipflops IC 21 ... 23 remain at high impedence.

The following pulse diagram shows the timing relationships for storage of maximum, minimum and check byte.

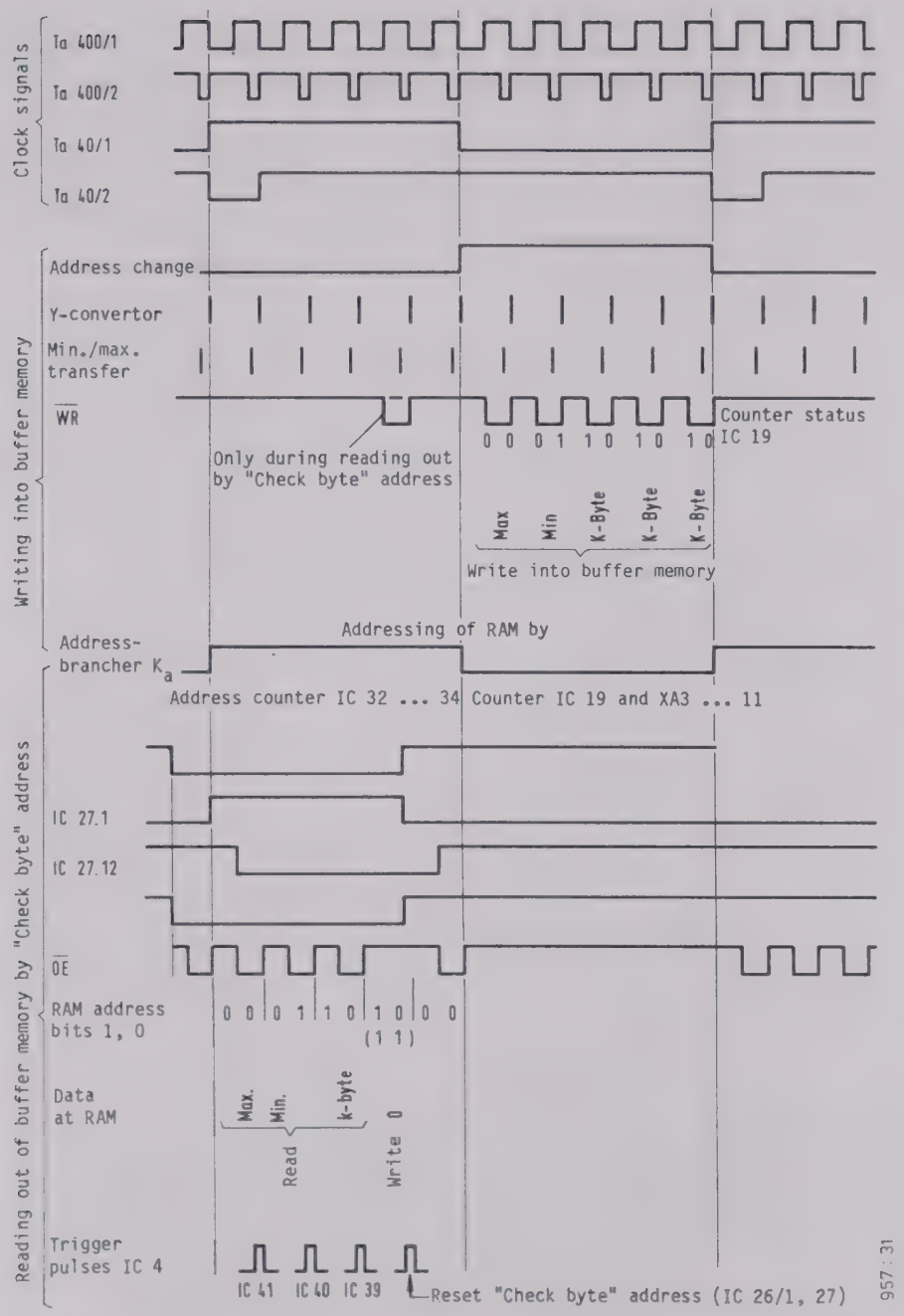


Figure 9-14 Pulse diagram

9.2.4.3 Reading out the buffer memory

In order to read out the contents of the buffer memory, the processor actuates the IO address "Check byte". Flipflop IC 26/2 is triggered. Signal "Ready" = L stops the processor. Signal "Check byte" is synchronized by the flipflops IC 27.

Reading out takes place whilst $\overline{\text{Ta 40/1}}$ = H; Ta 40/1 = L actuates the address changeover switch IC 35 ... 37 so that address counter IC 32 ... 34 determines the addressing of the RAM. Before actuating the IO address "Check byte", the processor can set the address counter to a particular value by means of the addresses "Set address counter/1" and "Set address counter/2". The address counter is enabled via IC 27.12 by the address "Check byte". During the reading operation it counts another four steps and successively addresses the storage locations for maximum, minimum and check byte which pertain to an X-value. Decoder IC 4.9 ... 15 decodes the two least significant bits of the address counter and successively triggers the registers IC 41, IC 40 and IC 39. Simultaneously, three pulses are switched through to the RAM input $\overline{\text{OE}}$ by IC 30.4 = IC 30.5 = H, IC 30.9 = L, IC 30.12 = IC 30.13 = H and IC 42.9 = H; the RAM reads out the data. (The RAM outputs are always active when there is no write operation/address change, erase check byte, clear memory in progress). The maximum is now in IC 41, the minimum in IC 40 and the check byte (bits 0 ... 3) in IC 39. The third step of the address counter - bit 0 = bit 1 = H - causes the RAM to be switched via IC 25.10 = L to writing in. If signal "Delete check byte" = H, the check byte is again addressed via two gates. Zero is written into this storage location (on account of R 22), and the check byte in the RAM is deleted. If the signal "Delete check byte" = L, the fourth unused storage location is addressed and the check byte in the RAM is not deleted. Decoder IC 4/2 resets flipflops IC 26/1, IC 27 and the reading operation is terminated.

By means of the IO address "Check byte", which prompts reading of the data pertaining to an X-value from the RAM, the processor simultaneously scans the check byte in IC 39. Subsequently, it scans the corresponding data in IC 41 and IC 40 via the "Maximum" and "Minimum" addresses.

9.2.4.4 The check byte

In addition to signals "V/$\overline{\text{D}}$(X)" and "Sweep out/$\overline{\text{return}}$", the check byte contains the information on how recently the values of maximum and minimum were updated. If new values for maximum, minimum and check byte for a particular X-value are to be written into the RAM by means of the signal "Address change", bit 0 of the check byte is set to H. This is performed by IC 23.14 = H. If the processor scans the storage locations using the address "Check byte", the check byte in the RAM is set to zero. If the processor scans these storage locations a second time before they are updated by an address change signal, bit 0 of the check byte is L. The processor thus detects that these are old values.

9.2.4.5 Clearing the memory

If the settings of the level meter or SG-4 are varied, the buffer memory is cleared. The processor, triggered by IC 26/1, actuates the IO address "Clear memory". Its output signal is synchronized by IC 27. IC 27.12 = L enables the address counter again. The address counter has already been set to the start address by the addresses "Set address counter/1" and "Set address counter/2". IC 30.3 = L always causes the address counter to be connected to the RAM via the address changeover switch. Together with the signal BA = H and the address "Inhibit memory" (D0 = H), IC 30.3 = L enables the write pulse for the RAM. The data bus of the RAM is kept at LOW by R 22, so that zeros are written throughout the RAM. When the address counter reaches the end of the RAM address range, address bit 11 (IC 34.2) becomes H. Flipflops IC 27 and IC 43 are reset. The address counter and the write pulse for the RAM are inhibited. The processor is stopped for the duration of the clearing operation ($\leq$ 5 ms) by "Ready" = L.

9.2.4.6 The clock generator

The clock generator consists of a crystal-controlled oscillator with T 1, T 2, two decade counters IC 13, three gates IC 14 and the flipflops of IC 15. The crystal Q_1 is operated in series resonance; T 1 is in a grounded-base configuration. The 4.194 MHz clock signal is picked off the collector of T 2 and subsequently divided down by IC 13. By means of IC 15, the clock signals are synchronized so that their transitions coincide in time. Present at the outputs of IC 15 are clock signals Ta 400/1 (419.4 kHz), Ta 400/2, Ta 40/1 (41.94 kHz) and Ta 40/2, as well as the inverted clock signals. See the pulse diagram of Figure 9-14.

9.2.4.7 Port assignments of the buffer memory card

See the following table (Figure 9-15).

Designation	Label Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Check byte	24	← free →					sweep out/ $\overline{\text{return}}$	V/D(X)	new value
Minimum	25	← binary coded →							
Maximum	26	← binary coded →							
	27								
Current value/1	28	← X-value binary coded →							
		XA 10	...					...	XA 3
Current value/2	29			sweep	← free →				
		XA 11	V/$\overline{\text{D}}$(X)	out/ $\overline{\text{return}}$	V/$\overline{\text{D}}$(Y)				
Current value/3	2A	← Y-value binary coded →							
		Y 7							Y 0
	2B								
Set address counter/1	2C	← free →		bit 7		binary coded			bit 2
Set address counter/2	2D	← free →					bit 10	bit 9	bit 8
Clear memory	2E								
Inhibit memory	2F								inhibit

Figure 9-15 Port assignments of the buffer memory card

9.2.5 PROCESSOR CARD CPU II circuit diagram (90) BN 965

9.2.5.1 Reset and power-off functions

When the 5 V supply voltage has been switched on, the processor is reset via CMOS gates IC 4, during the charging process of R 7, C 4. Additionally, the reset state is forcibly initiated as long as the POWER-OFF signal from the power supply has not dropped to LOW. If it is at LOW, i.e. the operating voltage has reached its setpoint value, the charging of R 6, C 3 must still be awaited. When the output of IC 4.6 ($\overline{\text{RESET IN}}$) goes to HIGH, the system starts.

If the processor writes in address 4, it resets FF IC 3 Q4 , so it forcibly initiates a reset. This state remains stable as long as POWER-OFF remains at HIGH (even with a decaying 5 V voltage).

FF IC 3 Q4 allows the POWER-OFF signal to be switched through to the TRAP interrupt.

Figure 9-16 shows the timing of $\overline{\text{RESET IN}}$ during the activation and connection phase. See also 9.2.5.5 for data saving.

To achieve the perfect system reset even during a brief switch-off, capacitor C 3 is discharged rapidly via diode Gl 1 during a self-reset, so that the full time constant of R 6 C 3 is always available upon switching on.

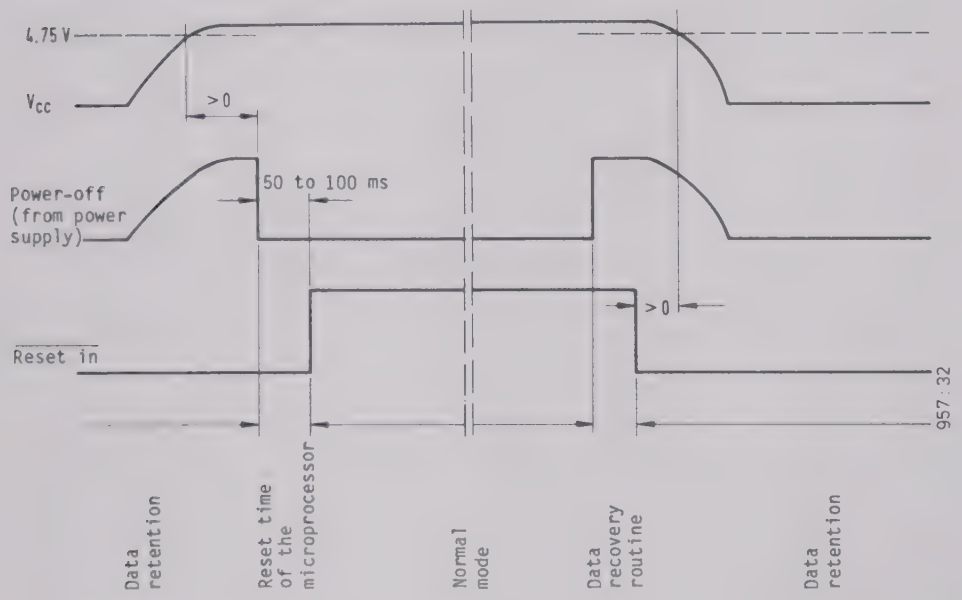


Figure 9-16 Reset function initiated by POWER-OFF signal

9.2.5.2 Clock signal generation

The 8085 processor has a one-chip clock oscillator. This operates with an 8 MHz crystal between pins IC 41.1 and 2. The 4 MHz clock signal is available at pin IC 41.37.

9.2.5.3 Latches, drivers and memories

Latch IC 40 accepts the addresses from the multiplex bus AD0-7 of the processor, so that the full address and data bus is available in parallel. This latch is loaded by the trailing edge of ALE. The address and data bus are wired to the connector for DMA applications or memory expansions.

The ROM and RAM buses are bunched separately and connected to the processor via drivers IC 30 ... 33 and IC 34, 37 respectively, in order to distribute the load presented by the memory. The separate buffering of the RAM is also required for data storage. See 9.2.5.5. For faultfinding, it should be noted that RAM address drivers IC 30 and IC 31 invert.

The strobe signals $\overline{RD}$ (= $\overline{OE}$) and $\overline{WR}$ are also buffered by driver IC 32.

Memory selection takes place via demultiplexers IC 35 and 1/2 IC 36, by means of which the memories are also deselected for IO operations or external $\overline{DISMEM}$. The corresponding bus drivers are included in the memory select/deselect by appropriate monitoring lines.

The select lines of the RAMs are wired via the analog switches in IC 25 which are closed in normal operation (see 9.2.5.5).

9.2.5.4 Monitoring lines

$\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$:

In normal operation, the processor monitors the data transfer by means of these 3 monitoring lines and the address and data buses. They are provided with pull-up resistors so that no inadvertent read or write pulses can be produced in the reset or hold states. $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$ can be operated externally in the hold state.

HOLD, HOLDA:

A HIGH at the HOLD input causes the processor to go to high impedence at the address and data buses, and at the monitoring lines $\overline{RD}$, $\overline{WR}$ and IO/$\overline{M}$. It signals this state by a HIGH at output HOLDA. When HOLD goes back to LOW, it continues its program. The LOW address latch IC 40 is switched to high impedence in parallel with the processor by HOLDA. Thus the card is DMA-capable. HOLD is a high-impedence input which must be driven in all cases.

READY:

A LOW at this input delays termination of the current read/write operation of the processor until it goes to HIGH again. It allows matching to slow memories or peripheral devices. The IO bus restraining element on the card and the arithmetic processor (AP), which is also provided on the card, use the READY in order to stop the processor until their operations are terminated. For this reason, the READY has a pull-up resistor R 10 and is connected via an open-collector gate to IC 11 by means of wired-AND with bus restraining element and the AP (see also 9.2.5.9 and 9.2.5.6). An additional restraint can be imposed via the strip plug connector, using external open-collector circuitry.

S0, S2, ALE, RST 7.5, RST 6.5, RST 5.5, SID, SOD

These monitoring lines or inputs/outputs are all wired to the strip plug connector and are only connected to processor IC 41 (except for ALE). See the INTEL data manual for functioning. Interrupt input INTR is not available and is grounded.

$\overline{CLEAR}$

With a negative pulse transition, this card input generates a TRAP interrupt via NAND-gate IC 5.13. This pulse transition at $\overline{CLEAR}$ can only pass when POWER-OFF is LOW or inhibit flipflop (IC 3, Q3) is HIGH. The user must ensure that, in the event of interrupt requests caused by $\overline{CLEAR}$, the TRAP is enabled by setting the inhibit FF IC 3, Q3 or by POWER-OFF LOW.

Irrespective of this, the LOW transition at $\overline{\text{CLEAR}}$ sets flipflop IC 3, Q 2 which can be read in via IO brancher IC 44. This facility was provided to allow the program to detect whether a TRAP has been initiated from the $\overline{\text{CLEAR}}$ input or by POWER-OFF. This so-called $\overline{\text{CLEAR}}$ flipflop is reset by writing in address 5 via demultiplexer IC 2. The AP is simultaneously reset (see 9.2.5.6).

The following are some internal monitoring lines on the card:

RWIO:

RWIO goes to HIGH during read or write operations in the IO area.

$\overline{\text{ERAM}}$:

$\overline{\text{ERAM}}$ (Enable RAM) selects the uppermost 8K of the addressing range provided for the RAM/AP.

$\overline{\text{ER3}}$:

$\overline{\text{ER3}}$ (Enable RAM 3) is the chip-select of RAM 3. When card input WITHOUT AP is HIGH, the uppermost 1/2 K addresses of RAM 3 are blanked and made available to the AP. In this case, ER3 is LOW from F800H to FDFFH.

WRRD:

This line (write or read) is the NAND combination of the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobe. It is HIGH with each read or write operation.

9.2.5.5 Data recovery (backup)

The CMOS RAM chips allow data retention (backup) in their quiescent state, at a low current consumption. Their supply voltages are therefore grouped separately for V_{bat} and led out for connection to a battery.

Figure 9-17 Connection between V_{bat} and 5 V voltage

In the switched-on state, diode G1 6 powers the RAMs from the 5 V voltage and charges a rechargeable battery.

Transition from normal to data retention mode:

A few milliseconds before the operating voltage drops below its minimum value, "POWER-OFF" is emitted by the power supply as a warning signal. If this is switched through to the TRAP, a non-maskable interrupt is triggered. In the remaining time, the processor is able to store important data in the non-volatile RAM. Subsequently, it sets an FF itself, the output of which toggles the $\overline{\text{RESET-IN}}$ signal to LOW (see 9.2.5.1). This causes analog switch IC 25 to open so that the chip-select inputs of the RAMs are pulled to V_{bat} by pull-up resistors R 17-20:

The RAMs are protected and no leakage current can flow into the remaining circuitry via the chip-select inputs. If the 5 V supply voltage finally disappears completely, all inputs/outputs of the RAMs are pulled to ground by pull-down resistors, thus achieving minimum current consumption. The RAM area is provided with additional buffering so that the pull-down resistors will not load the remaining system bus.

FF IC 4.6.9 generating the $\overline{\text{RESET IN}}$ and the analog switch IC 25 are at V_{bat} themselves and are therefore not affected by the drop in the 5 V voltage. The inputs of FF IC 4.6.9 are also kept defined by pull-down resistors.

Transition from data retention to normal mode:

The enable signal by POWER-OFF LOW is only emitted when the operating voltage has reached its setpoint value. When reset time R 6 C 3 has elapsed, CMOS FF IC 4.6.9 can toggle and the LOW at $\overline{\text{RESET IN}}$ is then removed. The processor starts and the analog switch switches through the RAM chip-select. See 9.2.5.1 for timing.

Checking the state of the battery:

Capacitor C 2 is at V_{bat} via R 3 and follows this voltage with the relatively great time constant

$$R\,3 \cdot C\,2 \approx 8\ s$$

Shortly after switching on, a check can be made to establish whether the battery voltage V_{bat} is above the limit of 3.2 V. Comparator IC 1 compares V_{bat} at C 2 with the reference voltage formed by R 1, R 2 from 5 V.

With the IO brancher switched over (UPW at LOW after writing into address 6), comparator output VRAM can be read in to bit 0 of the IO data bus.

Thus the processor can check the SG-4 so as to establish whether the battery voltage shortly before switching on was sufficient for data retention.

9.2.5.6 Demultiplexer IC 2

For controlling these card characteristics, five $\overline{\text{RS}}$ - FFs (IC 3/1 ... 4 and IC 6/3/4) are used; these can be toggled by means of demultiplexer IC 2 amongst other devices.

By writing into the address range of ROM 0, demultiplexer IC 2 becomes active and triggers the FF selected by the address, because its enable inputs are connected to the $\overline{\text{ROM 0}}$ select and the $\overline{\text{WR}}$ strobe. ROM 0 remains passive during write operations. It should be noted that address inputs A, B, and C are driven with the inverted RAM addresses $\overline{A_0}$, $\overline{A_1}$, and $\overline{A_2}$.

9.2.5.7 Free-running

If the settings of switches S 1/7 ... 10 are inverted, the processor cyclically addresses the entire memory area after a reset, rising monotonically. This allows bus lines to be monitored with an oscilloscope or signature analyzer. In order to examine ROM signatures, the corresponding ROM select (test points) must be used as a start/stop signal. Using switches S 1/7 ... 10 in conjunction with the pull-up resistors of the data bus and diode G1 2, reading of the commands of the bit pattern

7	6	5	4	3	2	1	0
H	L	X	X	X	X	X	H

is achieved during fetch-opcode cycles; these represent a subset of the 8085 command set and produce a program with continuous memory addressing.

9.2.5.8 IO bus

The 8085 processor possesses input/output commands with which a local IO data and address bus is served. This bus is normally utilized to control a device. So that these widely dispersed lines will introduce the least possible interference into sensitive circuits, a special bus concept is employed by W&G with the following features:

- Easily suppressable transients at CMOS drivers/receivers
- The address bus is always at a defined value and is only reassigned when necessary.
- During idle data interchange, the data bus is kept at the old value by the processor card.
- Special strobe signals allow the simple connection of address decoders and data latches/-drivers as peripheral devices (see 9.2.5.9).
- READY' input for arbitrarily restraining IO operations (see 9.2.5.9).
- Binary selectable restraining of the IO operations by inputs B_1-B_3 within specified limits (see 9.2.5.9).

The following facilities have been additionally created:

- The IO data bus can be short-circuited for diagnostic purposes, i.e. the data which have been output can be read in again by the processor whilst the connected periphery is kept passive by the monitoring lines.
- For special purposes (e.g. servicing) the IO read gate IC 44 and IC 45 can be switched over to read switches S 1/1 to S 1/6, the CLEAR flipflop (see 9.2.5.4), and the VRAM signal (see 9.5.2.5).

The IO addresses are transferred from the system bus by CMOS latch IC 39 and continuously output to external devices.

Output data are transferred from the system bus by CMOS latch IC 42 (when LSS is at HIGH) and switched to the IO data bus. This takes place both during an OUT operation of the processor and during an IN operation so that, after a read operation, the data bus can be presented with the same data as those just read in. By means of demultiplexer IC 2, a port area disable (PD) FF can be driven with complementary outputs $\overline{PD}$ and $\overline{PD}$. When the PD output has toggled to LOW, IO data driver IC 42 is activated continuously so that the data from driver IC 42 are read during an IO read operation, for diagnostic purposes. The output-enable input of IC 42 is pulled by $\overline{PD}$ to active LOW via diode G1 4 and is therefore connected to monitoring lines $\overline{RD}$ and IO/$\overline{M}$ via an OC gate IC 11.

Input data are presented to the system bus by latch IC 43 (with IO/$\overline{M}$ HIGH and RD LOW). This latch is loaded by the LSS (Low Speed Strobe) with the data from brancher IC 44, IC 45.

Brancher IC 44, IC 45 is set by flipflop IC 3 Q 1 and the flipflop itself is set by demultiplexer IC 2.

9.2.5.9 IO timing control

So that no IO bus conflicts are produced in an SG-4 by a delay of the address decoders, special strobe signals $\overline{RD}$', WR' and $\overline{LSS}$' (Low Speed Strobe) are generated on the card besides the IO data bus and IO address bus. $\overline{LSS}$ is combined with the other two strobe signals in a logic-AND operation.

Figure 9-18 Generating the $\overline{LSS}$ signal

Each IO operation consists of 3 intervals of time:

1. Addresses are valid: rise time for peripheral decoders
2. Strobe signal LOW: data transfer ($\overline{RD}$ and $\overline{WR}$)
3. Waiting period: decay time for peripheral decoders

The 3 intervals of time can be varied by the three card inputs B 1-3 (also independently of each other). B 1-3 represents a 3-bit number in positive logic:

$$n = < B\ 3, B\ 2, B\ 1 >,\ 0 \leq n \leq 7$$

This results in the following timing diagram for the IO strobe signals and the IO data bus and IO data address bus:

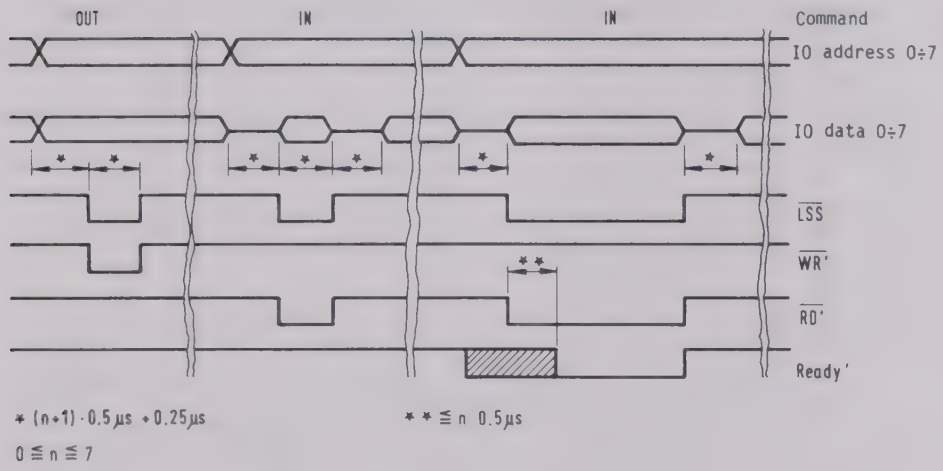


Figure 9-19 IO timing

Interval 2 can be extended to any length by READY' LOW.

Timing control sequence

FFs IC 8 and IC 9/1/2 are reset with the ALE signal. As soon as an address for the IO area is present on the data bus (IO/$\overline{M}$ = HIGH), the READY signal is thus placed at LOW via IC 10.8 and IC 11.4. Because the $\overline{load}$ signal (IC 7.11) is at LOW, counter IC 7 is already loaded with a value, e.g. OAH (n = 5). The clock signal for counter IC 7 is also enabled with READY. As soon as the counter has an overflow, FF IC 8/1/2 (Q = IC 8.5) is set with the next negative pulse transition. IC 9 (Q = IC 9.5) is connected in series as a shift register cell, so that the counter receives a $\overline{load}$ signal with the pulse transition following the next one.

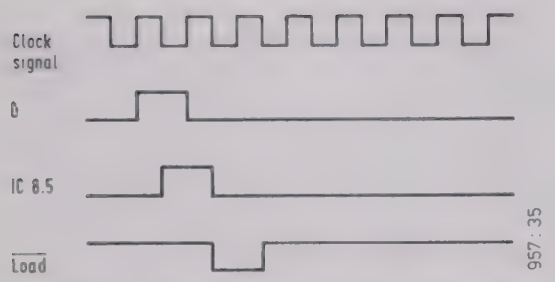


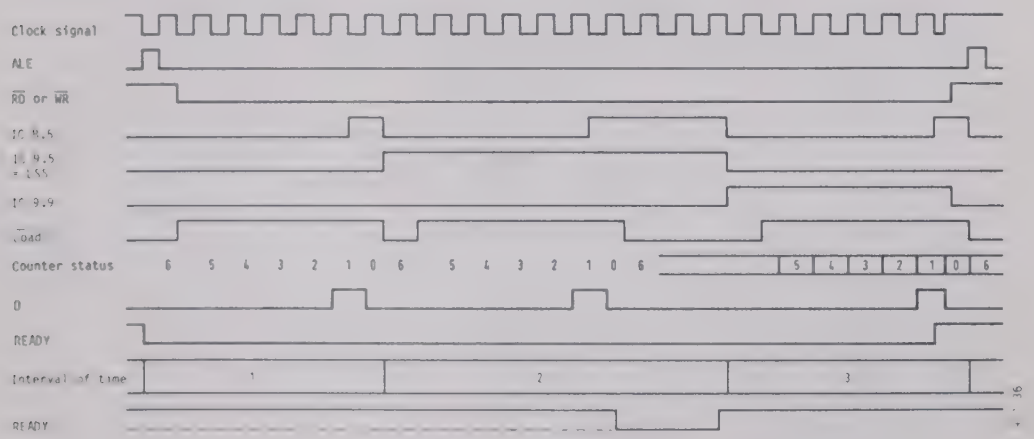
Figure 9-20 Signal sequence for counter overflow

This process is repeated for each interval of time.

At the end of the first interval, i.e. upon the first overflow, FF IC 9 (Q = Q 2 = IC 9.5 = LSS) is set. With the second overflow it is reset and FF IC 9 (Q = Q 3 = IC 9.9) is set.

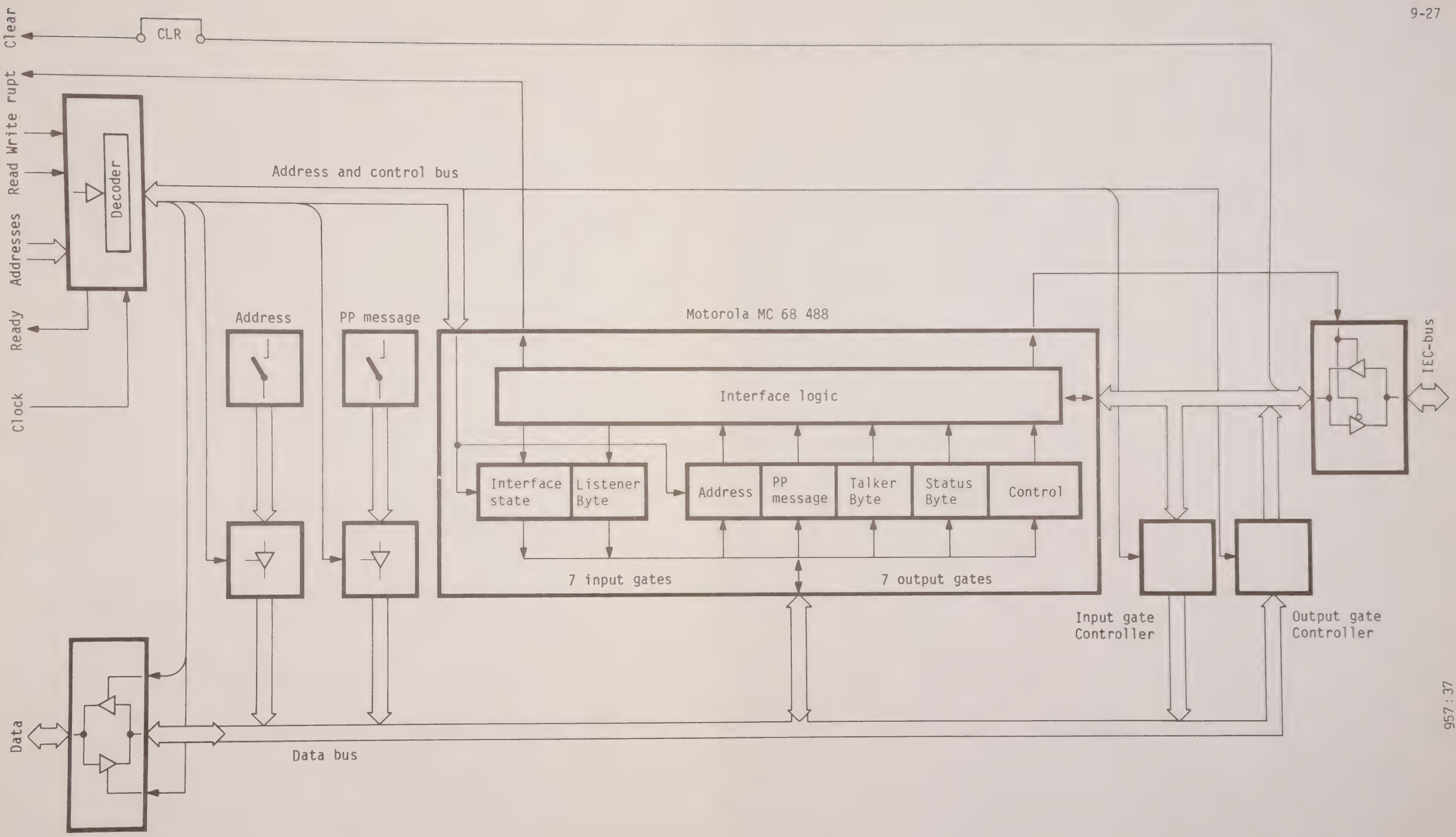
With the third and last overflow, the READY signal is then placed at HIGH (waiting state cancelled) via IC 10.8 and IC 11.4 and the clock signal is thus inhibited. The restrained process is therefore terminated.

Monitoring signal RWIO present at IC 9.10 resets IC 9 (Q = LSS) and simultaneously has a safety function: LSS pulses can only be generated when the processor intends to write or read.



Interval 2 can be extended to any length with READY'. Counter IC 7 is loaded with data B_1-B_3 at the start of each interval of time.

Figure 9-21 Sequences in timing control, general case



9-22 Block diagram of the <IEC 625> Bus card

9.2.5.10 Test points

2 x 8 test points are provided on the card:

Designation	Signal
$\overline{OE}$	output enable for ROMs, corresponds to $\overline{RD}$ strobe
ROM 0	chip-select of ROM 0
ROM 1	chip-select of ROM 1
ROM 2	chip-select of ROM 2
ROM 3	chip-select of ROM 3
ROM 4	chip-select of ROM 4
ROM 5	chip-select of ROM 5
ROM 6	chip-select of ROM 6
RAM 3	chip-select of RAM 3
RAM 2	chip-select of RAM 2
RAM 1	chip-select of RAM 1
RAM 0	chip-select of RAM 0
TP 4	$\overline{LSS}$ (Low Speed Strobe)
TP 3	$\overline{WR}$' (write strobe IO bus)
TP 2	SOD (serial output data from processor)
TP 1	$\overline{RD}$' (read strobe IO bus)

Figure 9-23 Test points

9.2.6 <IEC 625> BUS circuit diagram (91) BN 958

IEC Bus Interface BN 958 serves for matching microprocessor-controlled devices to the international standard interface bus <IEC 625> (abbreviated to IEC Bus).

9.2.6.1 Functional description on the basis of the block diagram

Shown in Figure 9-23 is the simplified block diagram of the <IEC 625> Interface Bus card.

The interface to the IEC Bus with the necessary driver and receiver circuits is on the right side.

Shown on the other side is the comb connection to the input/output bus of the internal microprocessor in the SG-4.

For the microprocessor, the IEC Bus interface represents a collection of input gates and output gates. The data interchange between IEC Bus and SG-4 takes place via these gates.

The data interchange between IEC Bus and SG-4 is controlled by the IEC BUS program. The PROMs in which this program is stored are not located on the IEC Bus interface card, but in the SG-4.

The actual interface logic is contained in the Motorola MC 68 488 IEC bus interface chip. This chip executes the majority of interface tasks independently, i.e. without support from the microprocessor in the SG-4; e.g. it participates independently in the IEC Bus handshake cycle and decodes all messages which are transferred on the IEC bus.

The interface states assumed as a result of these messages are written into the corresponding input gates.

Another input gate serves as transfer register for listener bytes. Listener bytes are items of data transferred from the IEC Bus to the SG-4, as long as the SG-4 is addressed as a listener, i.e. when setting parameters for the SG-4 are being transferred.

The chip contains output gates as well as input gates.

These serve

- to accept control commands with which the microprocessor can affect the behavior of the interface logic (e.g. in addition to many other possibilities, it can stop the handshake cycle or send a service request RSQ via the IEC Bus.)
- as transfer register for bytes which must be transferred from the SG-4 to the IEC Bus, e.g. talker bytes and status bytes. Talker bytes are items of data which are transferred from the SG-4 to the IEC Bus, as long as the SG-4 operates as a talker; e.g. when the measured result is being transferred.
  The status byte is the response of the SG-4 to a serial poll and contains the current SG-4 status.

The "Address" switch serves for selecting the SG-4 address.

The "PP message" switch is used to determine the data line of the IEC Bus on which the SG-4 is to send its status bit RQS (requested service), when the controller queries the status by means of a parallel poll.

To allow the IEC Bus Interface BN 958 itself to be used as IEC Bus controller, the internal microprocessor in the SG-4 must have direct access to certain IEC Bus lines. This access is possible via the controller input gate and the controller output gate.

Interaction between SG-4 and IEC Bus Interface

When the IEC Bus has reached a state requiring service by the internal microprocessor in the SG-4, the IEC bus interface sends an interrupt to the SG-4. As a result of this interrupt, the microprocessor then executes the IEC Bus program (see Figure 9-25). This is the case, for example:

- when the SG-4 is to be switched from local control to remote control or vice versa.
- when a listener byte has been transferred via the IEC Bus. The interface logic has then written this byte into the transfer register for listener bytes, and has stopped the handshake cycle. The handshake cycle remains interrupted until the microprocessor reads this byte (the IEC Bus line NDAC then goes to HIGH). After processing and storage of the listener byte, IEC Bus line NRFD is also set to HIGH.
- when the SG-4 must present a new talker byte. During writing of the new talker byte into the corresponding output gate, the handshake cycle is started by setting the IEC Bus line DAV = LOW.
- when the SG-4 is to be initiated for a measurement by means of IEC Bus command "Device trigger (GET)". The interface logic has then stopped the handshake cycle. It remains interrupted until the microprocessor has started the measurement and then enables the handshake cycle again (NDAC = HIGH and NRFD = HIGH).

- when the SG-4 is to be placed in a defined initial state by IEC Bus command "Device clear (DCL or SDC)". The interface logic has then stopped the handshake cycle also. It remains interrupted until the processor has placed the SG-4 in the initial state and then enables the handshake cycle again (NDAC = HIGH and NRFD = HIGH).

If wire jumper CLR is fitted on the IEC Bus Interface card, IEC Bus signal IFC (interface clear) prompts an initialization of the SG-4. This means that the SG-4 can still be initialized via the IEC Bus even in the event of a lockout. (This is important on SG-4s in unattended stations where an lockout caused by an external malfunction cannot be cancelled by switching the a.c. line voltage off and on again).

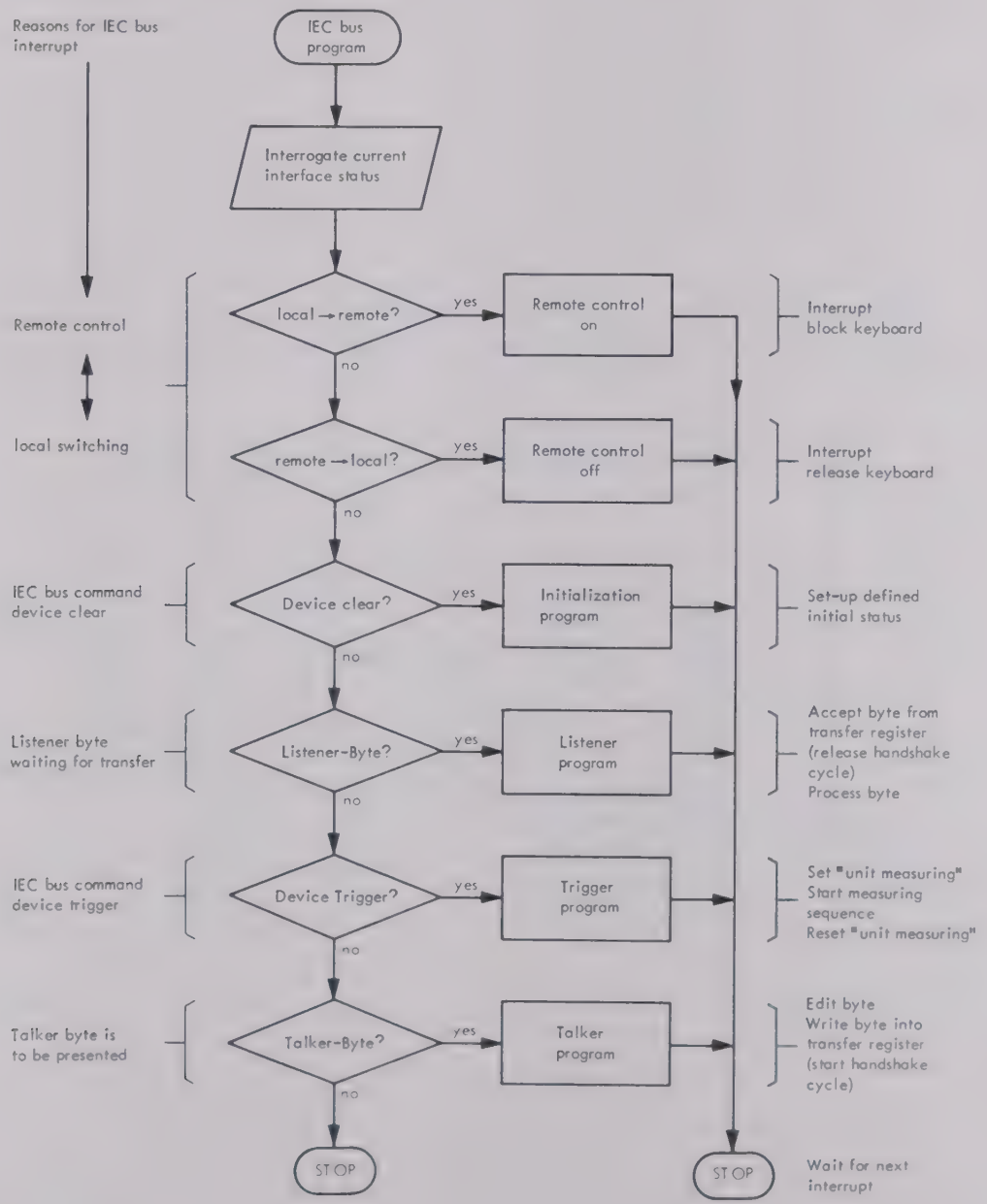


Figure 9-24 Structure of the IEC Bus program

9.2.7 CRT CONTROL CARD BSK-1 circuit diagram (92) BN 962

Before reading this circuit description, one should familiarize oneself with the following subjects:

- Driving a monochrome monitor according to the TV standard
- Characteristics of the GDP EF 9365/9366
- Basic operation of dynamic RAMs

Furthermore, knowledge of the following is assumed:

- TTL circuit techniques
- Simple transistor techniques
- Microcomputer techniques

9.2.7.1 Principle of operation

To produce a stationary image on a TV monitor, the entire image information must be stored in an image refresh memory (IRM). Whilst the beam is being passed across the screen, the IRM is simultaneously read out. The beam is blanked or unblanked, depending on the memory contents. In the simplest case, each pixel (image spot) on the screen is assigned a bit in the IRM. This principle is shown in Figure 9-25: the microcomputer system prompts the character and vector generator to structure the image information in the image refresh memory. The controller guides the beam via the blanking signal and addresses the memory bit which relates to the beam position (image signal). The 3 signal components are combined into a composite video signal in accordance with the standard and applied to the monitor.

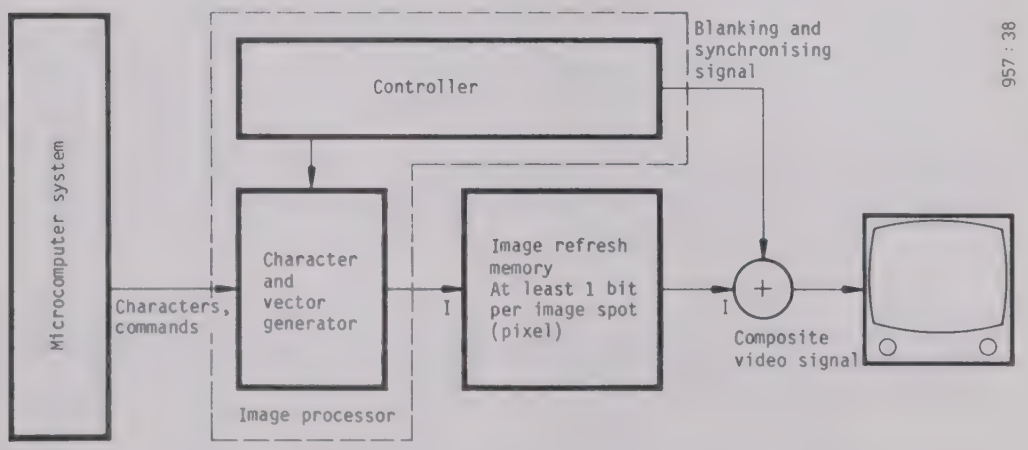


Figure 9-25 Spot-oriented monitor screen

9.2.7.2 Block diagram BSK-1

Shown on the right side is the circuitry for preparation of the composite video signal and the IRM with 3 memory banks. The image stored in bank 1 is represented with reduced brightness, and the image in banks 2 and 3 is represented with full brightness (memory bank 1 for graticule, for example, bank 2 for measured result and bank 3 for text). The image processor on the left side synthesizes the image information in the individual memory banks and normally also controls the displaying of stored images. By means of S 2, the display control for bank 3 can be transferred to a special addressing machine which allows magnification of the display. (The reason is explained in Section 9.2.7.3.). S2 to S8 can be directly controlled from the microcomputer via the output gate, so that the following can be determined by program:

- the memory bank in which the image information is to be stored (S3, S4, S5).
- whether the contents of a memory bank are to be displayed or not (S6, S7, S8).
- whether the contents of memory bank 3 are to be displayed in magnified or unmagnified form (S2).

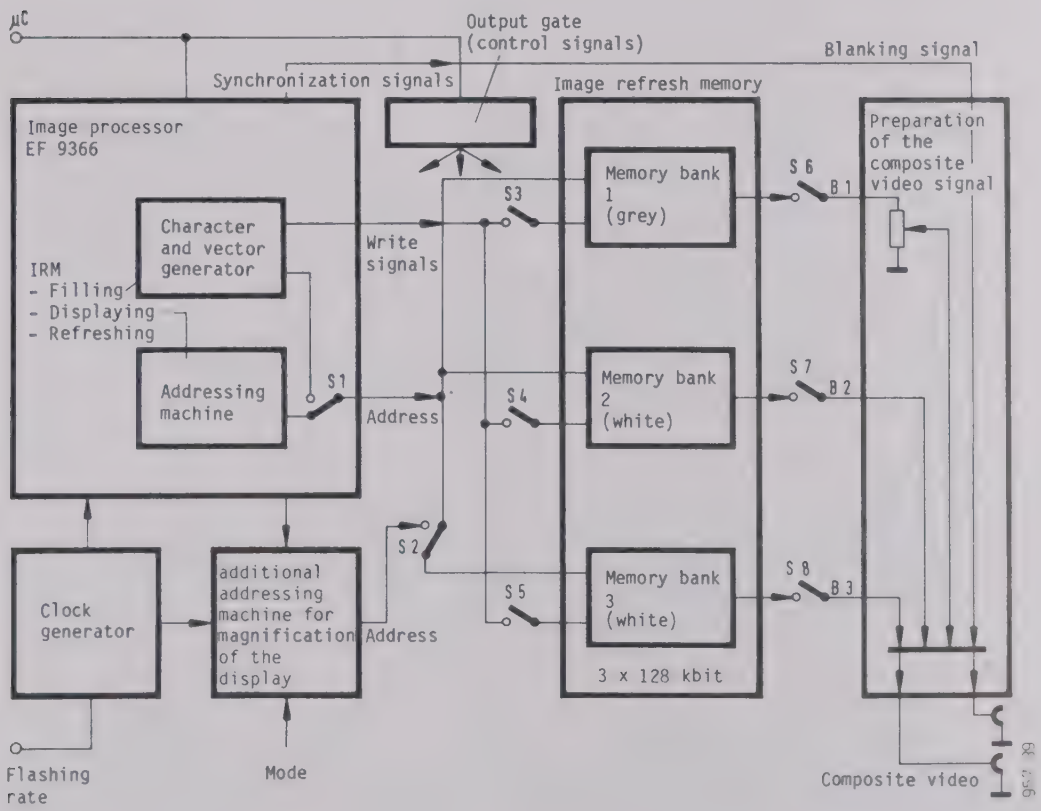


Figure 9-26 Block diagram BSK-1

9.2.7.3 Picture synthesis

Picture synthesis takes place without line interlacing, so that 312 scanning lines are produced. Of these, a maximum of approximately 302* are visible on the screen.

The memory banks of the IRM are organized into 512 x 256 pixels. Thus 46 scanning lines cannot be inscribed without special preparations. To create the well-proportioned picture, the image processor does not distribute the 512 points of the x-direction over the entire screen width, but produces an approximately square picture field in the middle of the screen. An unusable margin therefore remains at the sides.

* Application: this is a theoretical, maximum value. The number of lines which can actually be displayed depends on the time required by the monitor for the picture repetition. (Flyback blanking).

Subdivision of the screen area into zones

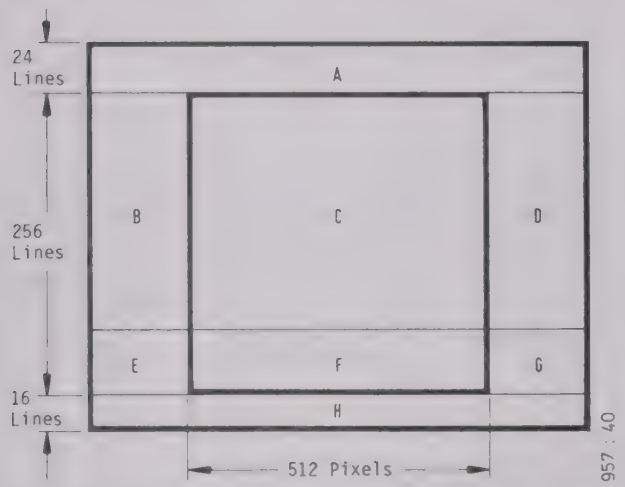


Figure 9-27 Subdivision of the screen area into zones

Assignments of the image refresh memory

Memory bank 1:

- Zones C and F
- Brightness adjustable between grey and white by means of preset potentiometer at end of card.
- Scanning 256 pixels in y-direction
  512 pixels in x-direction

Memory bank 2:

- Brightness white
- Otherwise as memory bank 1

Memory bank 3, mode 1 (unmagnified):

- As memory bank 2

Memory bank 3, mode 2 (magnified):

- Covers the entire screen
- Brightness white
- Each pixel in the image refresh memory is emitted twice to the screen (magnification in x-direction).
- Additionally, in zones B to G, each scanning line is beamed twice to the screen (magnification in y-direction).
- Thus the image refresh memory contains more pixels than can be displayed on the screen.

Memory bank 3, mode 3 (magnified):

- In all zones, each scanning line is only emitted to the screen once. Since, however, the IRM can only accept 256 screen lines, zones E, F and G cannot be addressed by memory bank 3.
- Otherwise as mode 2

The changeover from mode 2 to 3 is controlled via input $\overline{B3BA2}$ at the external addressing machine.

The characteristics of memory bank 3 appear non-systematic. However, they represent a good compromise between our requirements and the technical expenditure for implementation.

9.2.7.4 Circuit details

Microcomputer interface

The data bus of the image processor IC 60 and its address lines are directly wired to the slow bus of the microcomputer system. The remaining address lines of the bus system are connected at A_4 and E_1, E_2 and $\overline{E_3}$. Thus, when $A_4 = \overline{E_3} = 0$ and $E_1 = E_2 = 1$, the data strobe $\overline{LSS}$ is switched through to control input E at IC 60 (IC 58). The data direction is switched over with $R/\overline{W}$ at IC 60.

R 4 serves for matching IC 60 to the CMOS bus and to protect the inputs of IC 61.

If $A_4 = 1$, the data strobe $\overline{LSS}$ acts on the output gate (control gate) IC 61. Address decoding is incomplete (!): A_0 ... A_3 remain undecoded and no distinction is made between write and read operations. An incorrect read operation with the address of this output gate can therefore destroy its contents.

$\overline{INT1}$ is an OC output.

Counter chip IC 59 is counted up at 50 Hz by the VB output of IC 60. It can be reset by means of software via IC 61. In normal operation, it serves for generating the flashing interrupt (only one of the three outputs is normally wired in the card rack) and, in test mode, for synchronization between image processor and microcomputer (for description, see section entitled "Functioning of memory bank 3, modes 2 and 3 (magnified)").

Central clock supply

All processes on the BSK-1, which are not directly controlled by the microcomputer, are timed by the central clock supply. For this purpose, 8 other phase-locked clock signals are derived from a 14 MHz clock.

Principle:

OS1 generates a 14 MHz clock signal which is distributed in the circuitry by means of IC 66 and IC 56/2. Counter IC 2 is also counted through with this clock signal. Upon overflow, it is set to 0 or 8 depending on the sync' signal. The timing signals of the 8 derived clock signals required are stored in the PROM IC 3. The clock signals are stored in register IC 4 so that they are available in spikeless form.

Details:

With the same pulse transition used for storage of the clock states in IC 4, counter IC 2 counts further too. For this reason, the counter status and the address in the PROM are indicated separately in Figure 9-28: thus when the counter IC 2 is at 1, for example, the output of IC 4 is presented with the states which are actually assigned to the previous counter status and which are thus stored in address 0 of the PROM.

Each of the signal shapes in bits 1 to 5 is stored twice in the same shape, i.e. for counter status 0 to 7 and 8 to F. It is therefore sufficient to consider one half in each case.

- CK clock signal for IC 60 (image processor EF 9366). The status signals are additionally stored in IC 63 with the positive pulse transition.
- $\overline{RAS}$, $\overline{CAS}$ control signals for the dynamic RAMs (IRM). Both signals are inverted before they reach the RAMs. Thus they are stored in positive logic in the PROM (in negative logic in Figure 9-28).

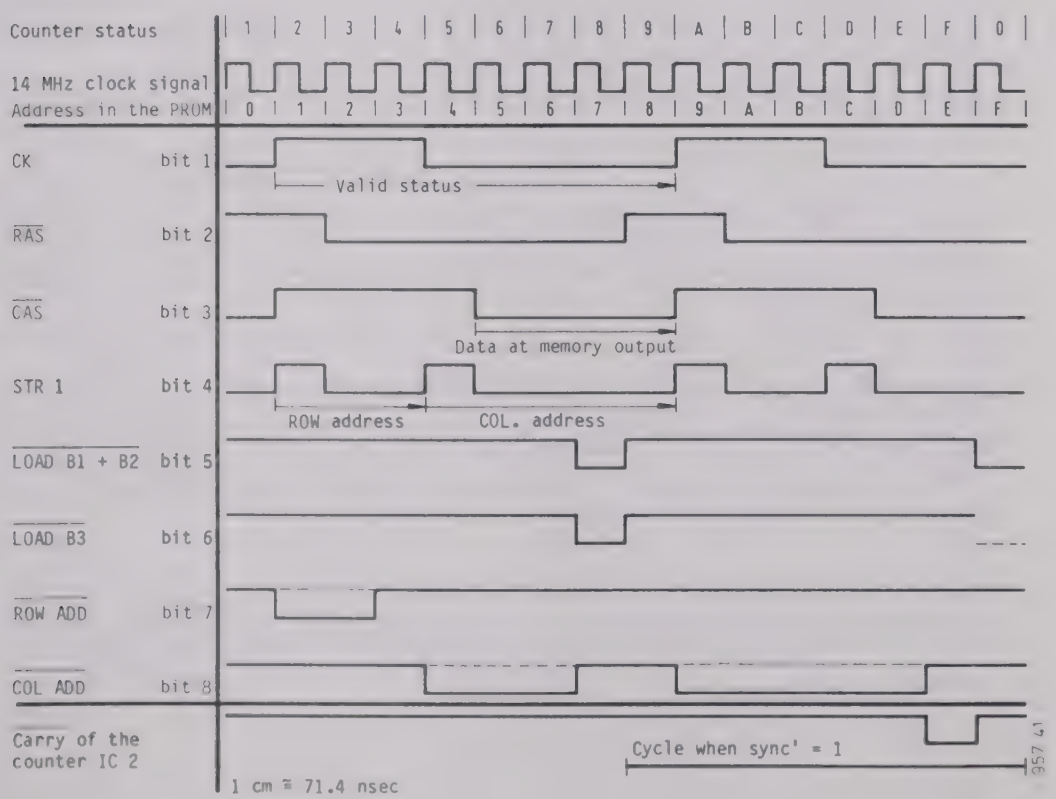


Figure 9-28 Central clock supply

- STR1 control strobe for address register IC 62. With the positive transition of the first pulse, the ROW addresses of IC 60 are buffered so that they are still valid after the leading transition of the $\overline{RAS}$ signal. This applies similarly to the second pulse and the $\overline{CAS}$ signal.
- $\overline{LOAD\ B1 + B2}$ characterize that the data at the output of the RAM of the IRM are valid.
- $\overline{LOAD\ B3}$, $\overline{ROW\ ADD}$, $\overline{COL\ ADD}$ control signals for memory bank 3. The signal traces drawn with solid lines apply to the modes with magnified display, and the dashed lines apply to the unmagnified case. The changeover takes place via input ADE at IC 3, i.e. via signal MAGNIFY. All the signal traces shown in Figure 9-28 are therefore stored twice in PROM IC 3 in reality: both the solid lines and the dashed lines. In both cases, addresses ADA (≙ A0) to ADD (≙ A3) are used in the same form so that ADE can be switched over with practically no interruption.

Functioning of memory bank 1 IC 9 to IC 18

- Write operation:

The status of IC 60 is stored in IC 63 with the positive pulse transition of the clock signal:

$MSL_0 \bullet\bullet\bullet MSL_2$	determine the RAM-IC within the memory bank in which the bit is to be written.
$\overline{ALL}$	= HIGH for write operations*)
$\overline{DW}$	= LOW for write operations
D_{IN}	= information to be written (1 bit)

Because $\overline{ALL}$' = HIGH, the POL input of IC 9 is at HIGH, so that the RAS in inverted form only reaches the RAM determined by $MSL_{0 \bullet\bullet\bullet 2}$ via E_4 of IC 9.

The memory bank which is opened for writing is determined by the microcomputer via control gate IC 61. For writing into memory bank 1, signal $\overline{DW}$' via IC 64 is only switched through to the RAMs of memory bank 1.

The data bit to be written in at DIN is applied to all RAMs present.

Before the selected RAM chip receives its $\overline{RAS}$, the corresponding address of IC 60 is applied to its address inputs via IC 62 and IC 1. This takes place similarly with $\overline{CAS}$, except that all RAM chips are selected.

- Read operation and display:

The pixels have a time interval of approximately 71 ns. Since the access time of the RAMs is considerably greater, all 8 RAM chips of one memory bank are addressed simultaneously, the data at the output are loaded into a fast shift register (IC 18) and fed from there to the monitor at high speed.

Status lines:

$\overline{ALL}$'	= LOW
$\overline{DW}$'	= HIGH

$\overline{E1}$ of IC 9 is HIGH. Thus RAS is switched via IC 8/2, and POL at IC 9 is switched simultaneously to all RAMs. At the end of the read access, therefore, there are 8 valid data bits at the inputs of shift register IC 18. The LOAD signal then appears at the output of IC 7/1 (cf. Figure 9-28), when the display is enabled by the microcomputer via $\overline{VIDEO\ B1}$ and when the beam is located on the core square (zones C and F) of the screen (BLK or BLK' = LOW). The image information is transferred into shift register IC 18 with the next pulse transition of the fast clock signal HCK.

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*) During clearing of the entire memory bank $\overline{ALL}$' can be LOW.

The output of IC 7/1 then goes LOW and the image information is applied to the preparation circuit for the composite video signal (IC 28, T 1 to T 5), bit by bit.

- Refresh:

The memories are organized so that the refresh during displaying is executed by the read operations. The refresh cycles additionally executed by image processor IC 60 are similar to read accesses. However, they remain invisible because BLK remains at HIGH.

Functioning of memory bank 2 IC 9, IC 19 to 27

Identical with that of memory bank 1

Functioning of memory bank 3 (unmagnified) IC 39 to 48, IC 30

The microcomputer sets $\overline{\text{DEHNEN}}$ (MAG) to HIGH. Magnification is thus switched off. As a result, Q_0 at IC 31 goes to HIGH and $\overline{Q_3}$ goes to LOW. $\overline{Q}$ of IC 33/2 is thus always HIGH and S 1 of IC 48 is always HIGH. IC 30 is always switched through. Except that IC 37/1/2 is switched through to the BLK' line, there is no longer any functional difference between this and memory bank 1. (The central clock supply of Figure 9-28 generates the signals drawn in dashed lines, i.e. $\overline{\text{LOAD B3}} = \overline{\text{LOAD B1 + B2}}$, $\overline{\text{COL ADD}} = \overline{\text{ROW ADD}} = \text{HIGH}$).

Functioning of memory bank 3, modes 2 and 3 (magnified)

Principle:

Via control line $\overline{\text{DEHNEN}}$ (MAG), the microcomputer releases the connection between memory bank 3 and the image processor IC 60. Of course, the clock supply via the central signal is maintained. However, addressing of memory bank 3 is transferred to an additional addressing machine (IC 32 to 35, IC 49, 50). Addressing in the X-direction takes place at half the clock rate and already starts at the beginning of each scanning line (magnification in the X-direction). Addressing in the Y-direction is sequenced with each or with every second scanning line. (Conditional magnification in the Y-direction). This mode can only be used for displaying memory bank 3. For writing, a changeover to unmagnified mode is made.

Details:

Since signal $\overline{\text{DEHNEN}}$ (MAG) intervenes in fundamental functions like the central clock generation, it cannot become effective at any time. It is synchronized in IC 31. Although the basic function of IC 31 is a shift register, it is only used for synchronizing the $\overline{\text{DEHNEN}}$ (MAG) signal: when $\overline{\text{LOAD B3}}$ is LOW, the state of $\overline{\text{DEHNEN}}$ (MAG) is transferred to Q_0 and $\overline{Q_3}$ with the positive pulse transition of HCK. If a mode with magnification is thus selected, then

- the address bus of memory bank 3 is no longer driven by the image processor via IC 30.
- the signals drawn with solid lines in Figure 9-28 are generated by the clock generation circuit. $\overline{\text{LOAD B3}}$ is thus only generated with every 16th pixel, the row address of memory bank 3 is switched to the address bus via IC 49 (signal $\overline{\text{ROW ADD}}$) and correspondingly, the column address by IC 34 (signal $\overline{\text{COL ADD}}$).

The second pulse of the $\overline{\text{COL ADD}}$ signal only creates clear states on the address bus during the leading transition of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, because it cannot be ruled out that the RAMs may develop malfunctions with resultant problems in signature analysis. Then:

- the load operation of IC 48 is no longer affected by BLK' (IC 37/1)
- IC 33/2 is activated.
- clock signal Ø/2 at S1 is switched to IC 48.

Thus every second clock pulse is a HOLD pulse, i.e. shifting only takes place with each second clock pulse transition. One "filling" of the shift register is therefore sufficient for 16 pixels.

The additional addressing machine:

The addressing machine esentially comprises two counters, the Y-counter (IC 35 "Line counter") and the X-counter (IC 50 "Pixel counter"). They are controlled by the image processor and by the central clock supply in such a way that their outputs can be directly utilized as an address for memory bank 3.

The X-counter is incremented once per storage cycle ($\overline{\text{LOAD B1 + B2}}$). Since, however, a new address is only required with each second storage cycle, output 1Q A (IC 50.3) is not used (magnification in the X-direction). At the end of a scanning line, IC 32/2 is set via the SYNC signal and IC 50 is thus reset.

The Y-counter is incremented at the end of each scanning line (no magnification in the Y-direction) or at the end of each second scanning line (magnification). Since the address bus is arranged in negative logic, considered logically this is a decrementing of the Y-counter. The most significant bit of the X-counter is used as counting pulse. If, therefore, the X-counter is reset at the end of the scanning line, the Y-counter receives a valid pulse transition. If signal VB = HIGH, all counting pulses are applied to Y-counter IC 35 via IC 36 (no magnification in the Y-direction). This is the case when the beam is located in zones A and H. If $\overline{\text{B3BA2}}$ is at LOW, IC 33/1 becomes active as a divider in the remaining zones (VB = LOW), and IC 35 is only incremented with each second line end (mode 2, magnification in the Y-direction in zones B to G). At the end of zone G, VB becomes HIGH and sets IC 32/1. This causes the Y-counter to be reset. Approximately 0.5 ms later, IC 32/1 is reset again via $\overline{\text{SYNC}}$. So that the next reset of IC 50, which only takes place now, will not apply undesired counting pulses to the Y-counter, this is reset in advance simultaneously with the Y-counter via the PRESET input of IC 32/2.

If $\overline{\text{B3BA2}}$ = LOW (mode 3), the y-counter has an overflow before it is reset via VB. A part of the picture would therefore appear twice on the screen. For this reason, FF IC 33/2 is set when IC 35 overflows and the display is therefore suppressed until the VB signal occurs (zones E, F, G).

During image change, on account of the vertical synchronization with leading and trailing pulses, the X-counter does not count far enough for 2 QC to be set. Consequently, upon reset, there are no negative pulse transitions at 2 QC and the Y-counter is not changed.

In magnified mode, the dynamic RAMs are sufficiently refreshed by the read accesses. Additional refresh cycles are not required.

Note relating to signal $\overline{\text{B3BA2}}$:

In the test unit, $\overline{\text{B3BA2}}$ is made switchable, but this input in the card rack of the SG-4 in which the BSK-1 is used is permanently set to LOW or HIGH.

Video output stage IC 28, I 1 ... I 5

The digital image signals and the digital synchronizing signal are combined into a composite video signal in the video output stage. There is no special blanking signal. Thus no distinction is made between blanking value and black value. During the beam flyback, the digital image information signals "black" in any case.

Transistors T4 and T5 form a push-pull output stage. In conjunction with R 14 and R 15, the two outputs BAS1 and BAS2 have an R_{out} of approximately 75 Ω. The ground of the composite video signal is wired separately and connected as a shield to the pins of the plug, immediately next to the composite video signals.

When T1, T2 and T3 are not conducting, the sync value is present at the output (R 9, R 12). When SYNC' becomes LOW, T 1 conducts and the output assumes the black value. If the "white" image signal arrives via IC 28/3 or IC 28/4, T3 conducts and the output value is presented accordingly. This applies similarly when T2 is turned on via IC 28/1. However, the effect on the composite video signal can be adjusted here by means of P1 (grey setting).

If an pixel is driven as "white" e.g. via IC 28/4, practically no increase in brightness can be expected when "white" is additionally driven via IC 28/3. Thus T 3 practically reaches its minimum forward voltage with a "white signal". This applies similarly when "grey" and "white" (T2 and T3 conducting) are driven simultaneously.

Diodes Gl 1, 2, 3 are intended to prevent saturation of the transistors (acceleration).

The luminance signals are clocked at 14 MHz via IC 56/2 and IC 28/1/3/4. Vertical and horizontal lines on the screen thus appear with about the same brightness. Additionally, this prevents the sync value of the composite video signal from being falsified (IC 56/2) during the sync pulse by an image signal which can theoretically appear via IC 28/3.

Test mode IC 66, IC 59

In various tests it is necessary for all sequences to be controlled not only logically, but also with precise timing by the microcomputer. With TP 1/3 ($\overline{TEST}$), the fast clock signal can be switched to the read clock signal $\overline{RD}$ of the microcomputer via IC 66. The STOP signal is activated in IC 66 with the same changeover. In this mode, of course, no display on the screen is possible, nor can the contents of the dynamic RAMs be considered as being reproduceable. For faultfinding, however, using signature analysis in the major part of the circuitry, this mode is ideally suitable.

After the changeover to test, all processes on the BSK-1 occur slower by a factor of approximately 12. When output VB of image processor IC 60 goes to LOW, the first FF of IC 59 toggles. The STOP signal at IC 2 then becomes effective via IC 66 and inhibits all other processes until IC 59 is reset again from the microcomputer, and the process is repeated. In this way, the stimulus programs in the microcomputer and the sequences on the BSK-1 are synchronized.

For the SYNC signal, IC 66 is configured as a simple invertor.

9.2.8 7" MONITOR circuit diagram (93) BN 980

9.2.8.1 General description

The 7" monitor BN 980 processes composite video signals (image signal with blanking and synchronization and composite video signal) with 1 V_{pp} into 75 Ω with a line duration of 64 µs, and 50 or 60 Hz frame frequency. Images with 296 lines (frame) or 592 lines using the interlacing method can be displayed. In general, the P.C.B. is also suitable for 24, 28 or 31 cm CRTs (picture tubes).

The P.C.B. is arranged in 5 functional groups:

1.) Video amplifier
2.) Horizontal sweep circuit
3.) Auxiliary voltage generation
4.) Vertical deflection circuit
5.) CRT with mask and any "soft keys"

9.2.8.2 Video amplifier

The video amplifier has 2 equal inputs. Its rise time can be adjusted with C 48 and C 49.

Brightness and contrast can be adjusted with a d.c. voltage (0 - 5 V), and a brightness potentiometer (P 7) is already provided on the P.C.B..

The video preamplifier supplies synchronizing pulses at one output (IC 3.15) and, at a second output (IC 3.10), the video signal which is preamplified depending on contrast, and shifted in absolute position depending on brightness. This is amplified in the video output stage (T 3 and T 4). Diode Gl 9 provides protection against saturation as well as protecting the CRT from excessive cathode voltages. The load resistor for the output stage is R 43.

9.2.8.3 Horizontal sweep circuit

The horizontal sweep circuit is of the type used in monochrome TV receivers. It operates with energy recovery.

The supply voltage is built up to 25 V so that the line output coils can be driven directly. The linearity control (L5), picture width control (L4), line output coils and tangential correction capacitor (C 29) are directly in series with the output transistor (T 5) and kick-back capacitor (C 30). When T 5 turns off, the voltage over C 30 rises, the magnetic energy from the sweep coils and line output transformer is transferred to C 30 and a magnetic field of inverse polarity develops. (C 30, C 29, line output coils, L 4 and L 5 form a resonant circuit). Once the maximum field strength is reached, a negative voltage would develop at C 30. This is prevented by an kick-back diode (integrated in T 5), so that the resonant circuit is only formed from C 29 and line output coils L 4, L 2 for the sweep. A faster flyback is thus achieved in relation to the sweep. The losses are compensated for from the supply voltage via the line output transformer.

T 5 is driven by the integrated circuit TDA 2593 (IC 2). This requires a composite video signal with positive synchronizing pulses, which are applied via pulse shaper network R 32, C 24, C 15, R 21. The line frequency is determined by C 21 and R 27 and should be aligned to the nominal value (e.g. 15.625 kHz) with no input signal. When the line kick-back pulse (via R 41) and composite video signal are present, the line frequency is synchronized with a PLL circuit. (PLL filter R 24, C 19 or, for "Fast regulation time constant" C 17, R 23, R 24, C 19.) The fast regulation time constant is automatically selected during adjustment. It can also remain switched on permanently, and this is advisable for operating the monitor with video recorders. For operation with the CRT control card, the slow regulation time constant should be selected because in this case the line synchronizing pulses are not equidistant during picture change.

By injecting a current at IC 2.5, the phasing of the horizontal pulses can be varied so that the picture on the monitor is shifted to the right.

A synchronizing pulse for the picture change is available at IC 2.8.

9.2.8.4 Auxiliary voltage generation

The voltage pulse during the line flyback is subjected to various stages of transformation in the line output transformer, so that the following are available after rectification:

65 V for the video output stage
-65 V for the background adjustment
400 V for the first accelerating voltage, and
11 kV for the second accelerating voltage.

For the 11 kV, the CRT acts as a smoothing capacitor. The diode is potted in the line output transformer.

CAUTION: AFTER SWITCHING OFF, THE HIGH VOLTAGE REMAINS STORED IN THE TUBE!

For the vertical deflection, the booster voltage of 25 V is available across C 34.

Since the -65 V are clamped to +12 V (C 36), the tube is blanked when the operating voltage is switched off.

9.2.8.5 Vertical deflection circuit

The heart of the vertical deflection circuit is formed by IC 1 (TDA 2653). With no input signal, the oscillator runs at 46.6 Hz. In the deflection process, the frequency is determined by C 2, R 7, R 8 and P 2. For the flyback, R 8 and P 2 are short-circuited and a higher frequency is thus selected briefly. This was necessary in order to ensure a picture flyback within 1 ms (1.5 - 2 ms for TV sets). This oscillator drives a sawtooth generator whose amplitude is affected by P 1, R 3 and C 1 via T 1. The frequency detector in IC 1 detects whether the frame frequency is 50 Hz or 60 Hz and compensates via R 2 for the picture amplitude errors created by various frame frequencies. The sawtooth voltage is applied to IC 1.3 via a buffer stage. On the one hand, it is averaged by an active lowpass filter ($f_{cut\ off} \approx 2$ Hz), so that the average direct voltage of the sawtooth is present at the output of IC 4. On the other hand, the sawtooth is applied to a bridge (consisting of R 11, R 14, R 15 and R 76). The preamplifier is arranged at the bridge diagonals. Thus any ripple is not transferred via C 7 into the linearity of the vertical deflection.

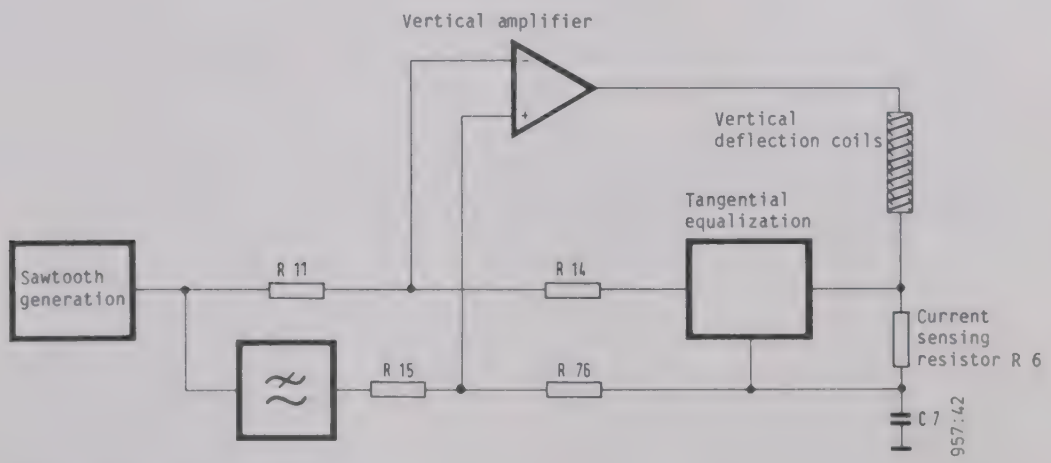

Figure 9-29 Vertical deflection circuit

The deflection current is picked off at R 6 and fed to the vertical amplifier IC 1.4 via arm R 14/R 11 of the bridge.

To achieve a faster vertical flyback, the operating voltage for the output stage IC 1.5 is built up to 50 V by the kick-back generator via C 3 for the duration of the flyback. This pulse is also utilized for blanking during the picture flyback (R 50, R 56).

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Wandel & Goltermann GmbH & Co
Post Box 45 · D-7412 Eningen u.A. · Telephone 891-1 · Telex 729 833